A real time electronic emulator with realistic data generation for reception tests of the CMS ECAL Front-End boards

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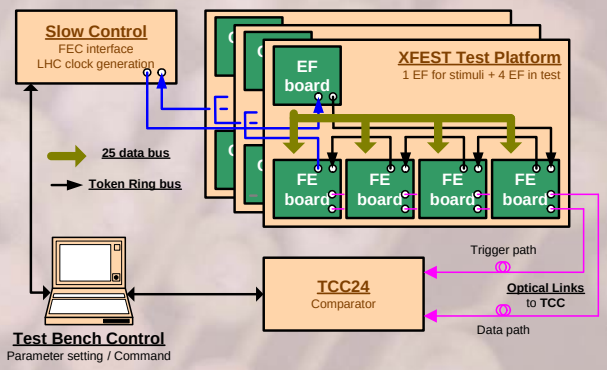
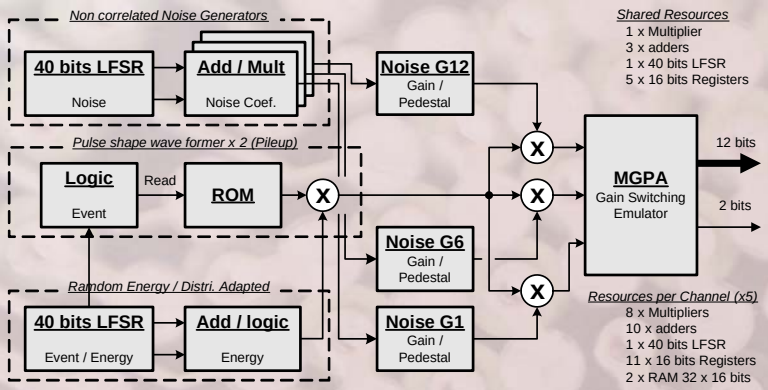
XFEST (eXtended Front-End System Test) Test Bench

Designed to test the *3132 readout Front-End boards (FE) of CMS/ECAL* sub detector. Test validation is obtained when Data and Trigger outputs of the board under test are strictly identical to those of a well known reference card for about one hour (10^{13} patterns).

- Built to test as much as 12 FE boards at the same time, by *set of 4 boards*
- Same digital input patterns are sent at a rate of 40 MHz onto all FE boards
- To emulate the 25 digital input vectors, a FPGA prototype version of the FE board is used in reverse mode (EF) for realistic data generation
- The outputs of the FE boards under test are shipped by optical fibres to a prototype Trigger Concentrator Card (TCC24) equipped with FPGA
- Real time comparison of the FE outputs, is performed using the embedded TCC24 FPGA for the Trigger and the Data path



Block Diagram of XFEST Test Bench



Block Diagram and Resources of a single PATGEN channel

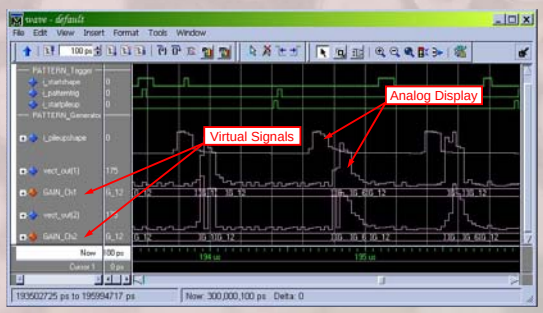
Pattern Generation Solution

FE prototype board including 7 FPGA devices of one million logical gates, is used. *Fully digital model* designed to emulate the digital input vectors from Very Front End electronics. Realistic and versatile data generation with:

- I²C slave interface for internal parameter access
- specific statistical signal amplitude model
- programmable range of signal amplitude
- digitally coded waveform stored in ROM
- pileup capability
- non correlated noise for the 3 VFE gains
- fully programmable seed for noise sources
- fully programmable value for noise, pedestal and gain
- MGPA dynamic gain switching emulator
- start/stop function under software control

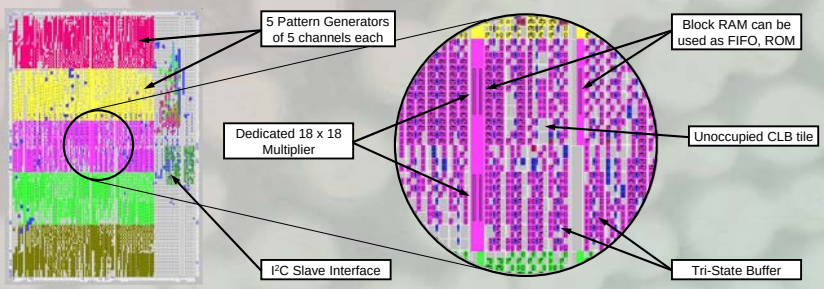
Simulation Phase

- Analog display of successive digital values
- Implementation of virtual signals for efficient debug
- HDL resource package for testing:
  - → statistical signal amplitude model
  - → I²C slow control access



Implementation Phase

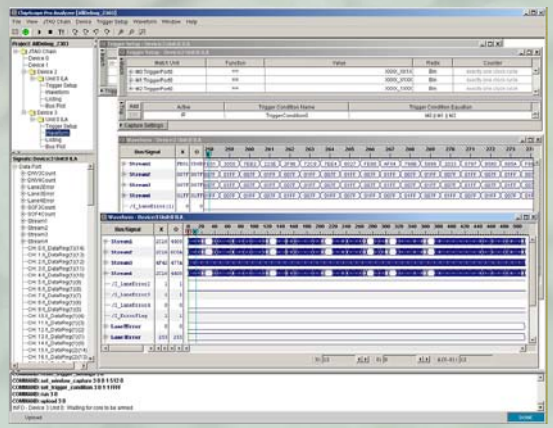
- Needs high arithmetic block count: *41 multipliers, 53 adders*
- IP generator to implement resources
- Pipeline architecture for complex function, e.g. signed multipliers
- HDL Generic parameters for hierarchical concept (block conception)
- Floor-planning process to reduce cell placing and routing time
- *860.000 equivalent gate count* and a die occupancy ratio of 70%



Trigger and Data Path Analysis

On each path, a FPGA checks that received data for every channel are the same. Dedicated solutions have been adopted to aggregate and compare data from different clock time domains, in an unique clock domain:

- Internal input blocks RAM are configured as self-addressing FIFO buffer
- 'Automatic data align' mechanism is used for more than one *set* in test
- Analysis of real time data entries is performed to avoid buffer controlling
- 'On the fly' parameters are detected and extracted from data block format
- Parameter setup is controlled through an embedded VME interface
- Diagnostic and access to error counting are included in designs
- Internal debug solution based on 'ChipScope-Pro' software is adopted



ChipScope-Pro windows with 'TRIGPATH' (on the front) displaying an error on channel 3 and 'DATAPATH' waveform (behind)

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