Toward a m³ DHCAL prototype
with an integrated readout

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Warsaw
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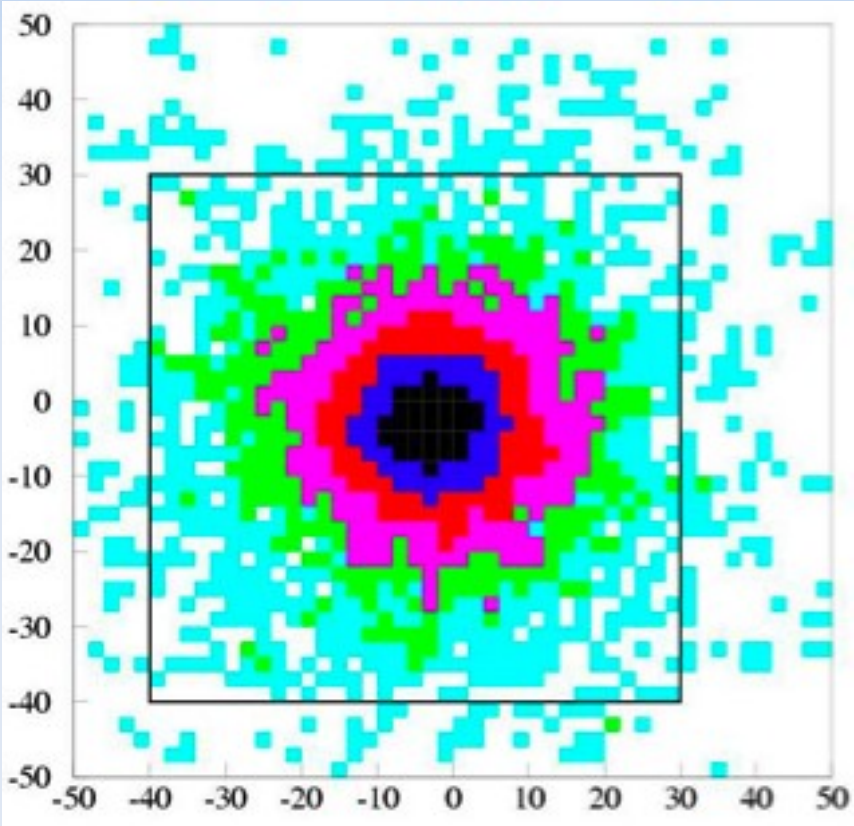
Overview

- Case for a digital calorimeter
- Detectors :
  - µMEGAS
    - Characterisation
  - RPC
- Digital Readout by ASICs
  - HARDROC
  - *DIRAC*
- Integration & Debug Card: DHCAL1 & readout
- Cosmic tests

- 1 m² prototype
  - Validation of large surface detector & readout
- 1 m³ prototype
- First use new gen. of EUDET DAQ2
  - see V. Bartsch talk
- *Efforts of integration in ILD & SiD*
  - *Mechanical & simulation*
  - See corresponding talks

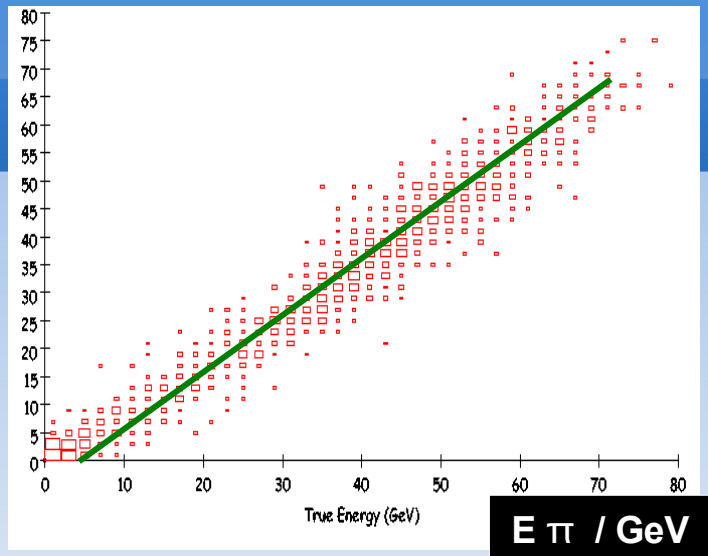
Case for a Digital HAdronic CALorimeter

- 1 or 2 bits of information per cell
  - Finer granularity → 1×1 cm² × 40 planes
    - Ideal for a **PFA** approach
  - Cheaper, simpler, more robust detectors
    - GRPC, µMEGAS, GEM's
- Gaseous detectors
  - insensitivity to neutrons
    - narrower showers (99% of hits in 70×70 cm² for 100 GeV π)
    - suppression of big fluctuations
- Recovery of information ?
  - counting
    - improvement: 3 thresholds
  - topology
    - clustering



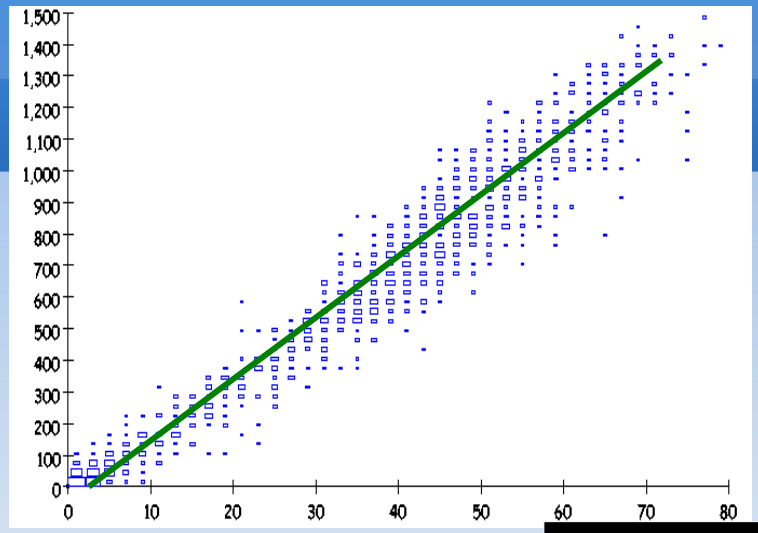
See note LC-DET-2004-029

Edep



E π / GeV

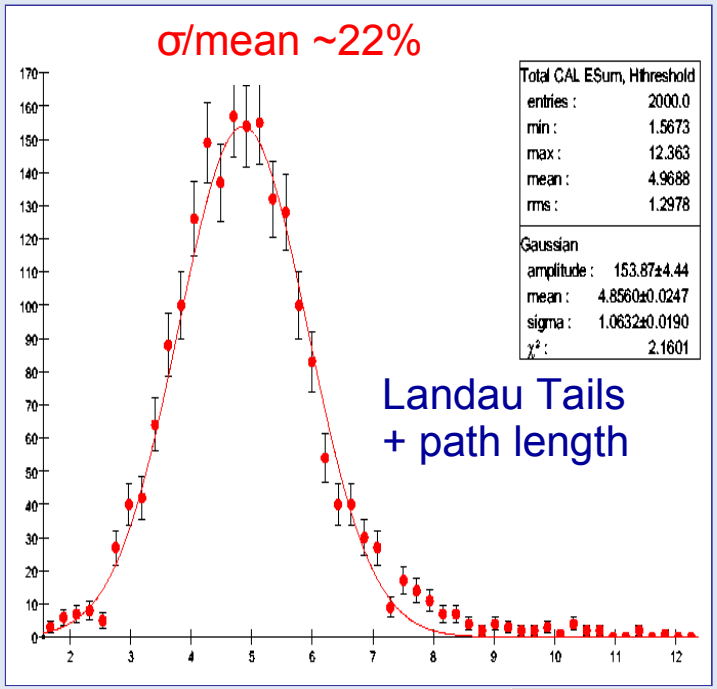
N hits



E π / GeV

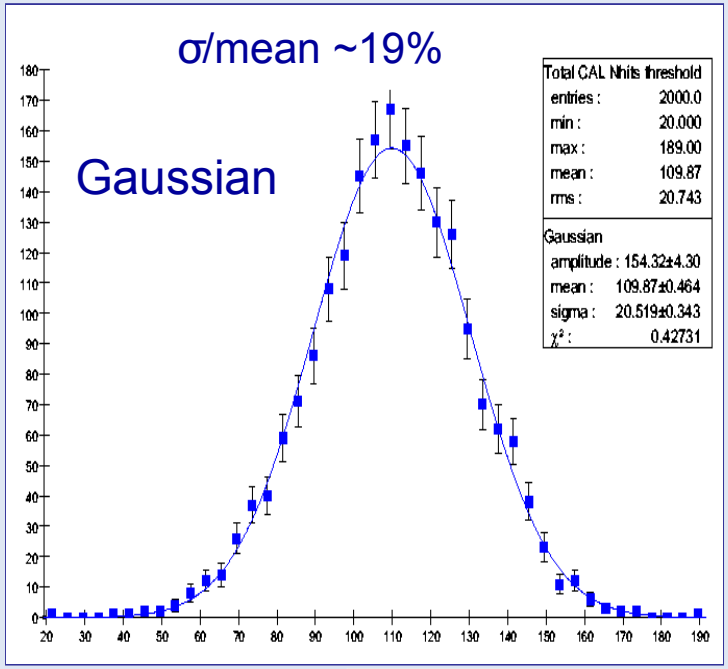
Simulation Calice

Analog



E / GeV

Digital-1bit

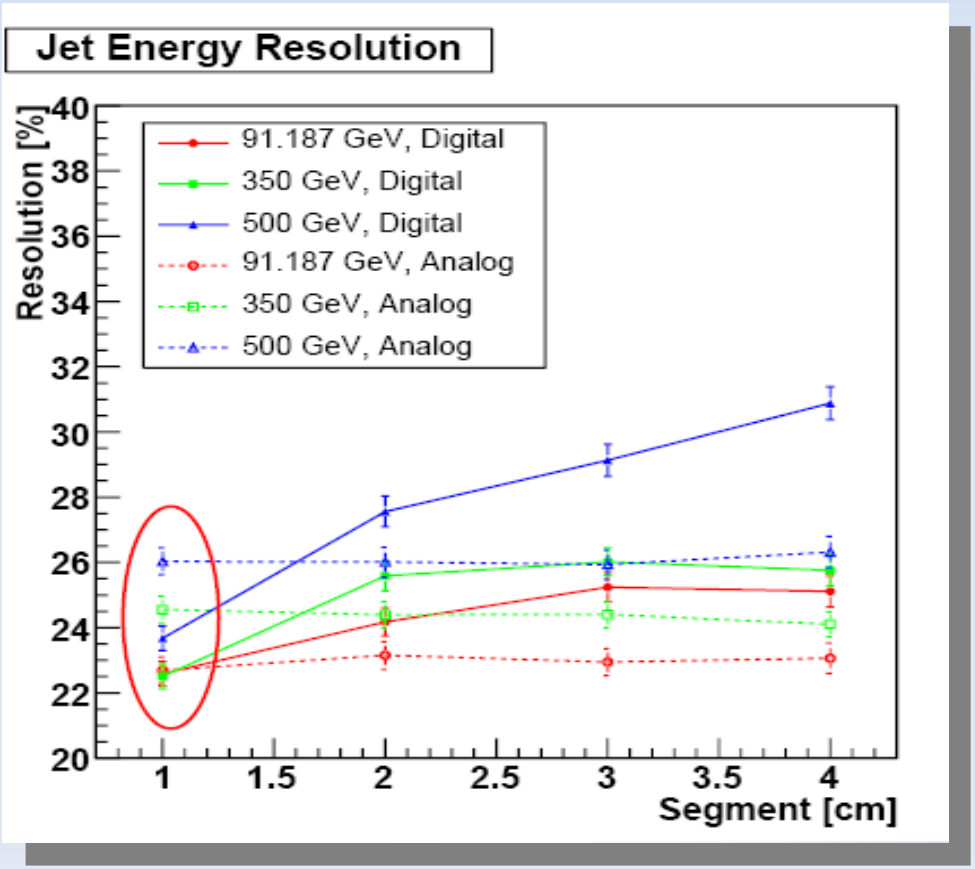


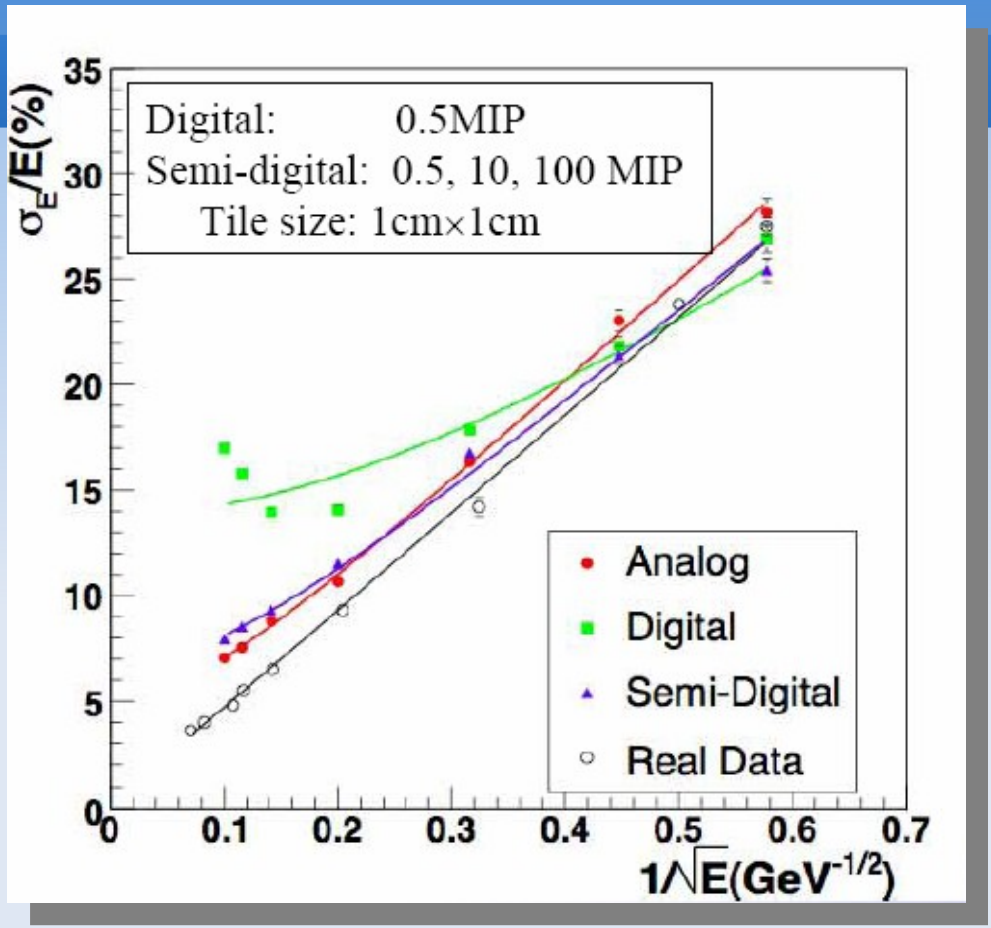
Number of hits

π⁺ 5 GeV

Resolution studies

- GLD HCAL study by KEK Group
  - 3 thresholds (0.5, 10, 100 MIP's)
  - 1×1 cm² tiles
- 1 bit better @ low E





- $e^+e^- \rightarrow qq$ (uds)
  - $\sqrt{s}$ = 91, 350, 500 GeV
- Assuming Perfect PFA
- → Better jet resolution

H MATSUNAGA
Pramana J. Phys., Vol. 69, No. 6, December 2007

DHCAL's in the Calice Collaboration

- **USA**: **See pres. of J. Repond**
  - GRPC / GEMs
  - Physics prototype
  - Binary (1 bit) R/O
- **EUROPE**:
  - GRPC / µMEGAS
  - Technological prototype
    - embedded RO electronics
  - Semi digital R/O

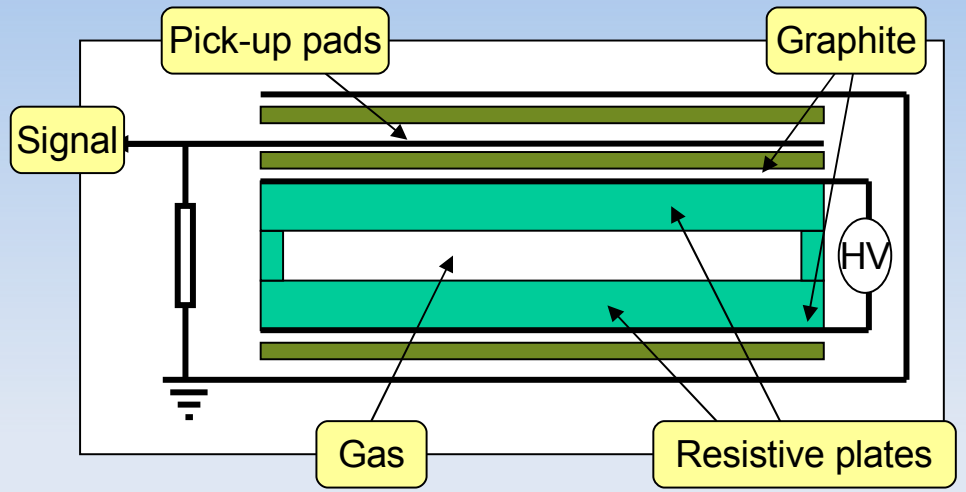
- France, Russia, Spain

  CIEMAT, IHEP, IPNL, LAL, LAPP, LLR
- ~25 persons
- Funding:

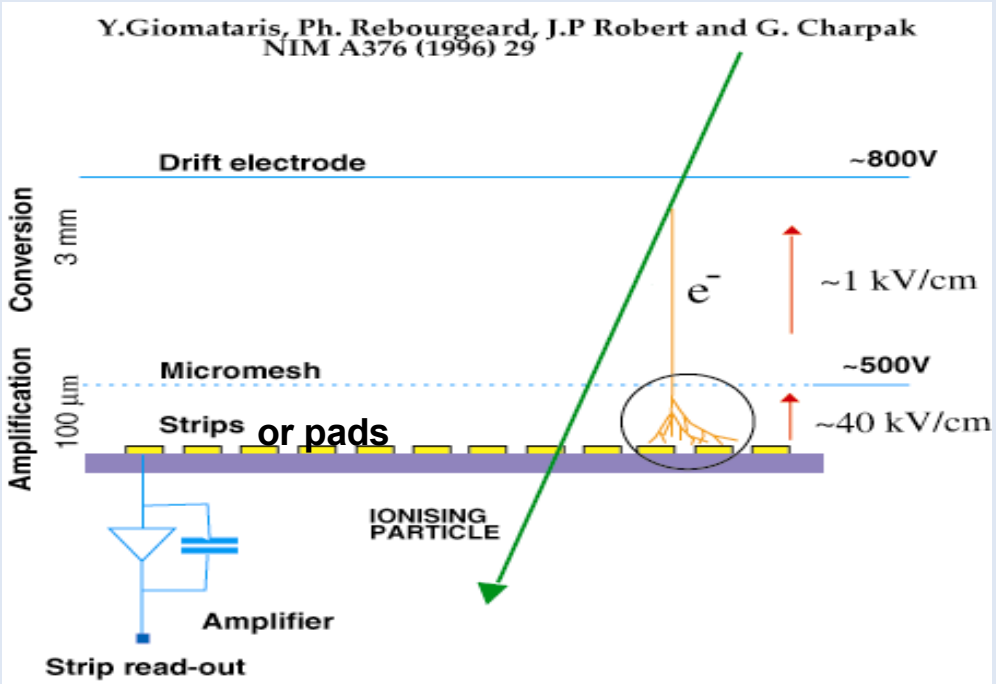
  CNRS/IN2P3 + EUDET + French ANR

Gaseous detector technology

- Detectors
  - GRPC *(IHEP+IPNL)*
    - simple, robust, rate ≤ 100 Hz/cm²

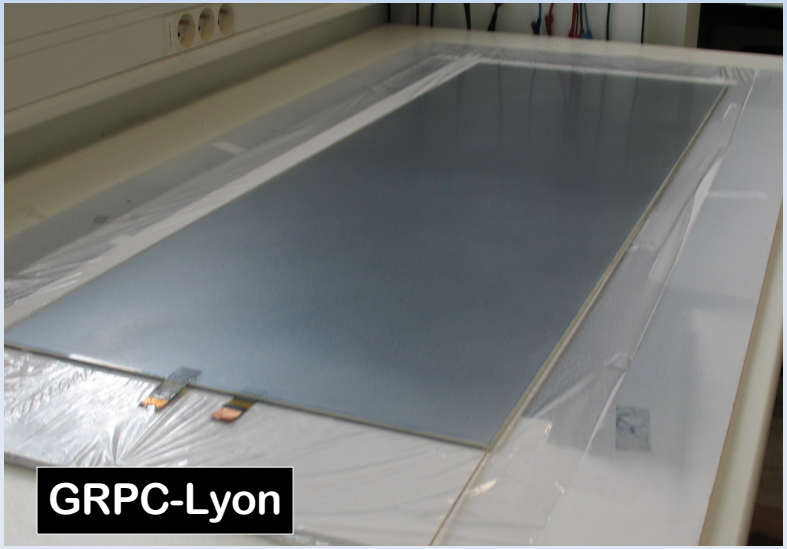


  - µMEGAS: *(LAPP)*
    - robust, high rates, delicate implementation

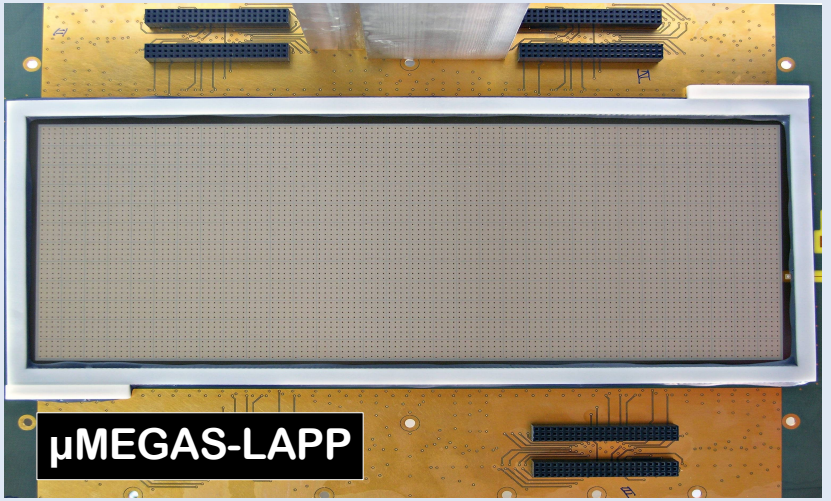


Detectors: prototypes

- GRPC:
  - 8×8, 32×8, 50×32, 100×32, 100×100
    1 cm²-pad : already produced and tested.

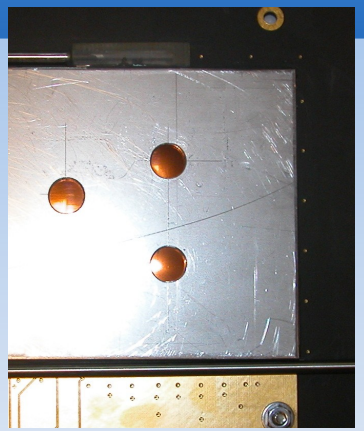


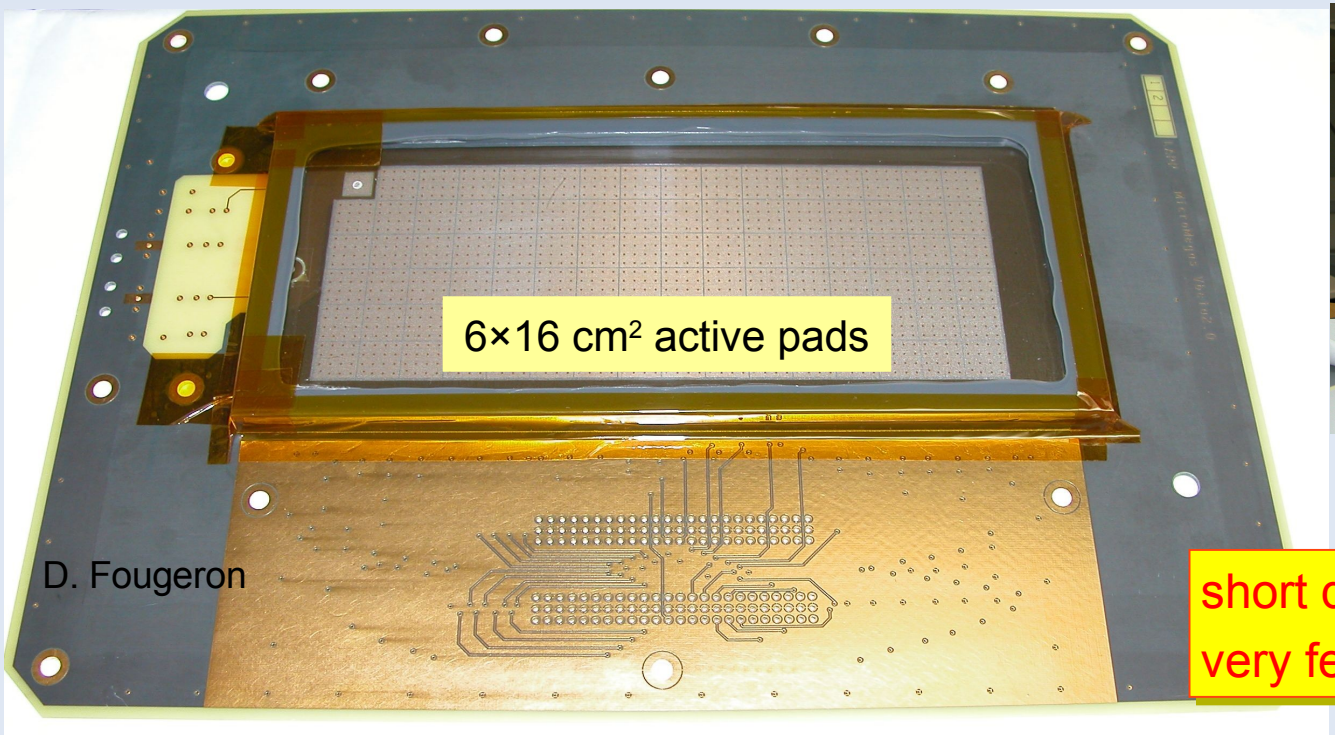
- µMEGAS:
  - 16×6, 32×8, 32×12
    1 cm²-pads: produced and tested.
  - Larger size detectors are under development



µMegas Prototypes

- PCB rooting with great care (4 layers)
- Stainless Steel top with holes for X-rays
- 5 µm thick copper drift cathode
- Chamber assembly in clean environment



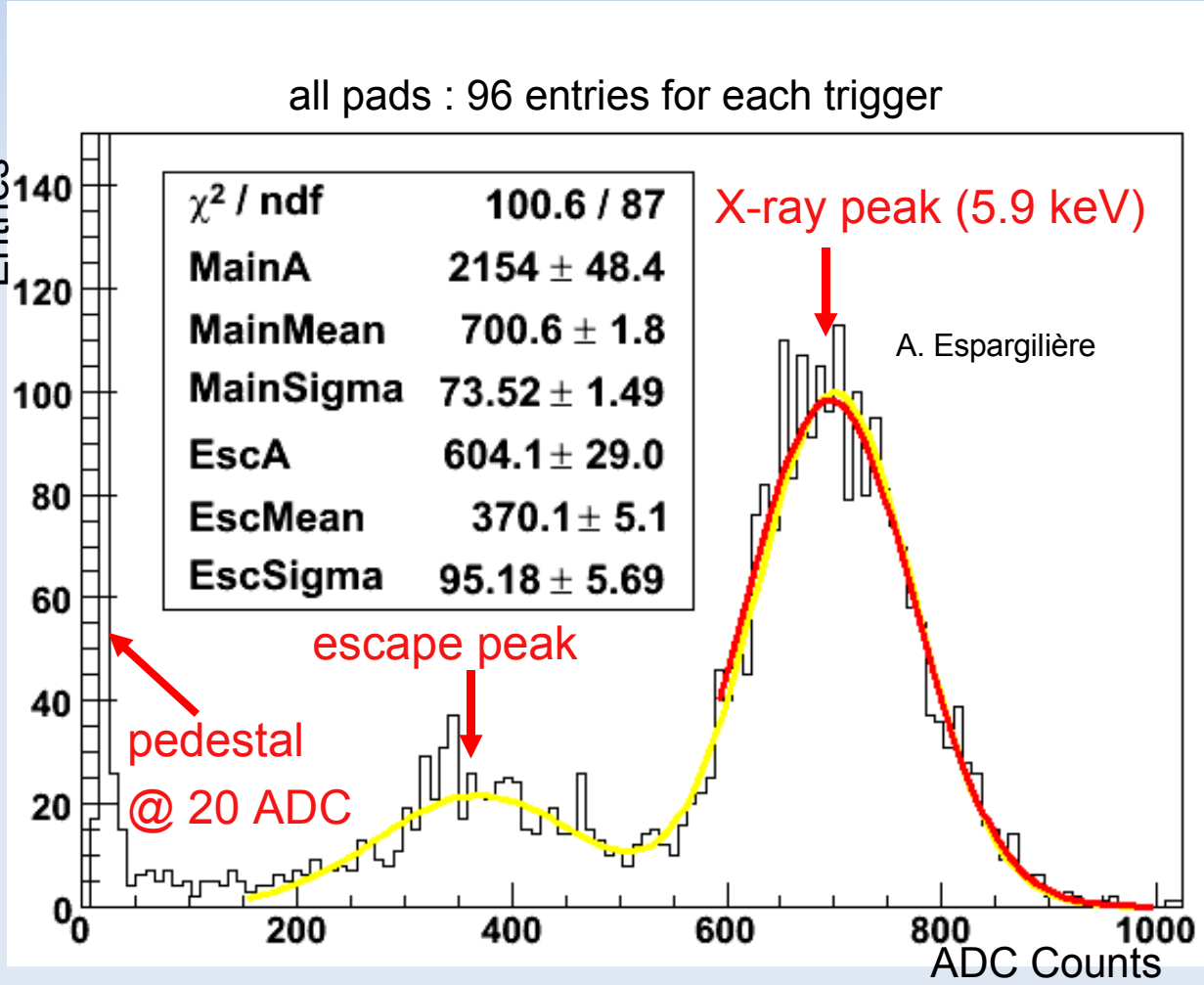


short dust burning time !
very few sparks during functioning

µMEGAS: X rays response

- ^{55}Fe source (5.9 keV ≈ 228 e- in drift volume)
- Trigger on mesh : preamp (T output) + fast ampli

V_{mesh} = 420 V
V_{drift} = 470 V
E_{mesh} = 35 kV/cm
E_{drift} = 167 V/cm

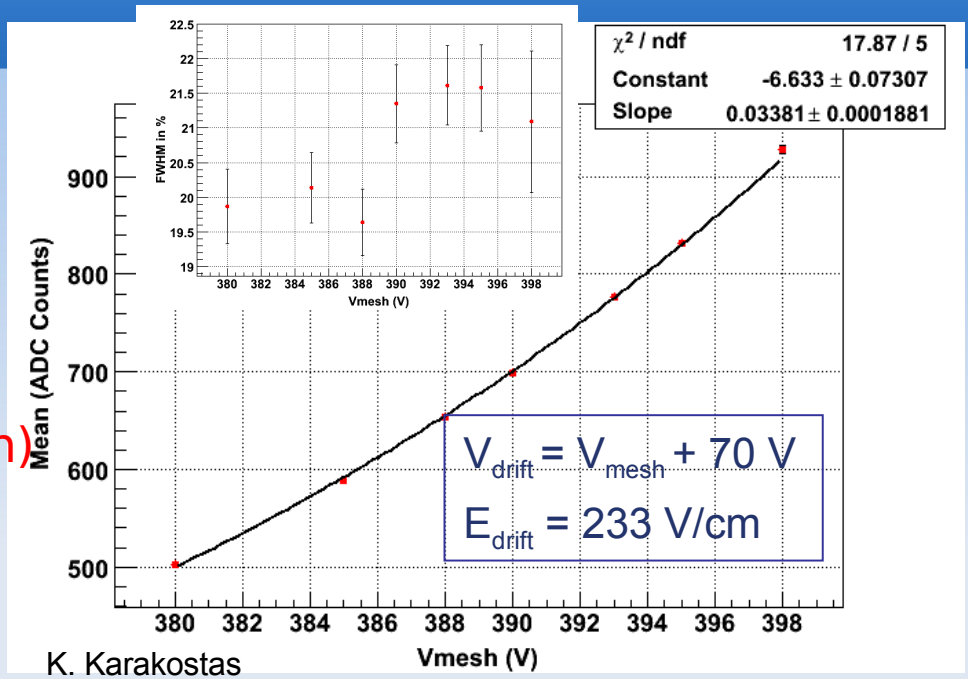


Gassiplex Readout :
Peak = 680 ADC cnts
= 996 mV
≈277 fC
Gain ≈7600
FWHM = 25.5%

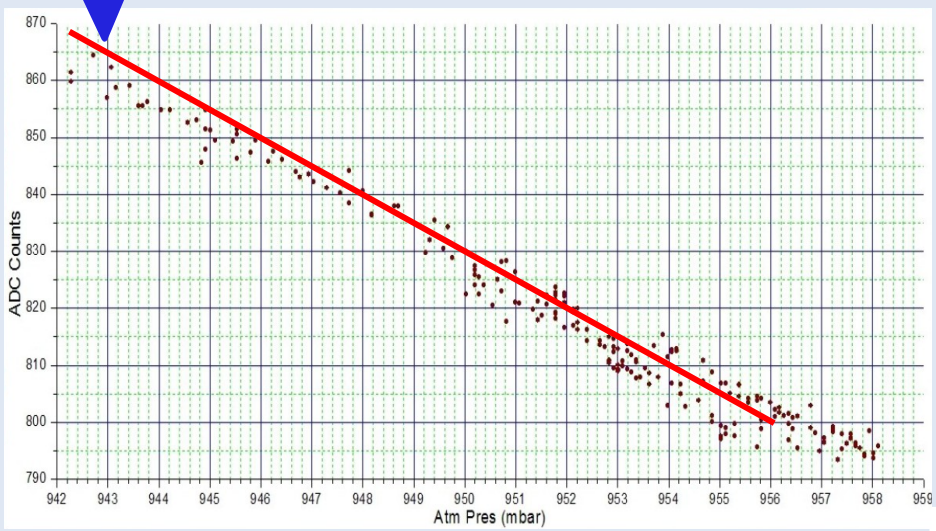
T2K(same techno) :
FWHM = 26%

µMEGAS: X rays response

- vs V_{mesh}
  - expected exp. behaviour
- vs V_{drift} and Gas flow dependencies
  - Saturates for Flow > 0.20 l/h (7 vol/h)
  - Gain ↘ when Drift field ↗
- Stability vs atm pressure
  - Slope = - 2 fC/mbar



K. Karakostas



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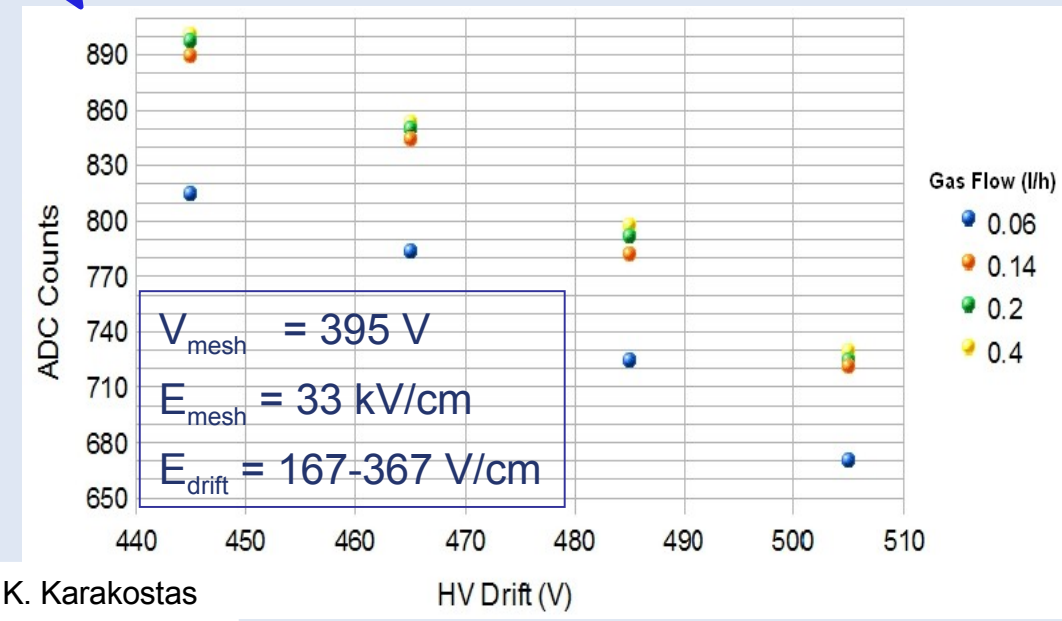
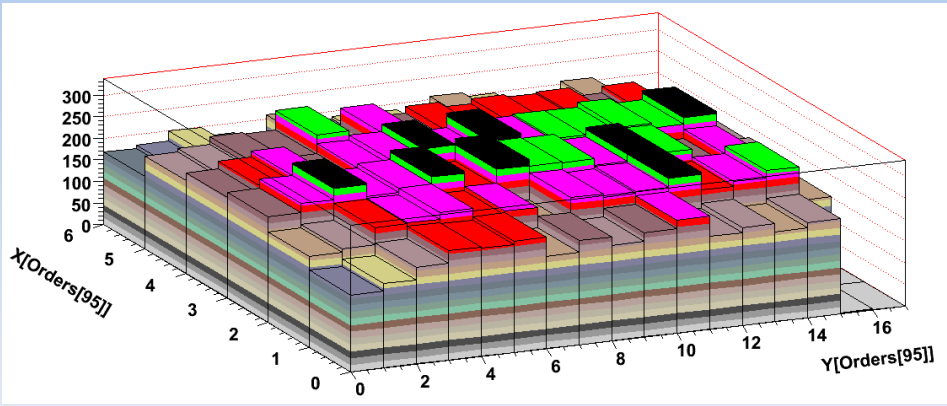


K. Karakostas

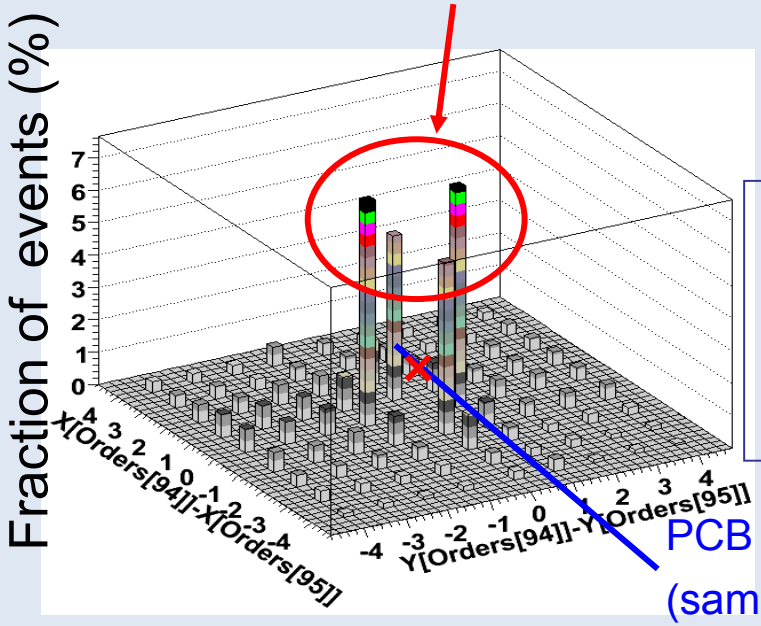
µMEGAS: X-talk from Cosmics

- Trig on 3 scint. coinc.
- MIPs selections:
  - Charge ~ 32 fC
    Gain ~ 6900
- X-talk:
  - 20% of events have events to highest E pad

Chamber mapping (geographic occupancy)

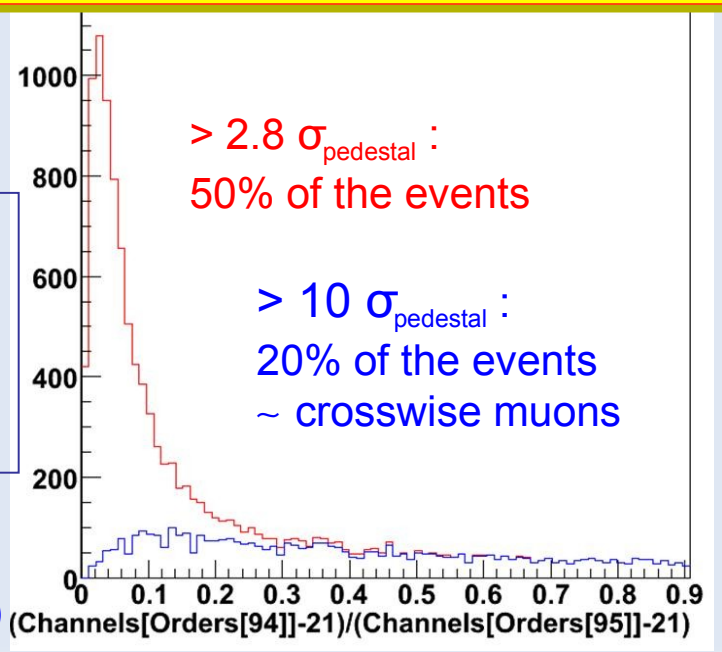


Signal(second pad) / Signal(muon pad)



V_{mesh} = 410 V
V_{drift} = 470 V
E_{mesh} = 34 kV/cm
E_{drift} = 167 V/cm

PCB routing along X
(same Y than muon pad)

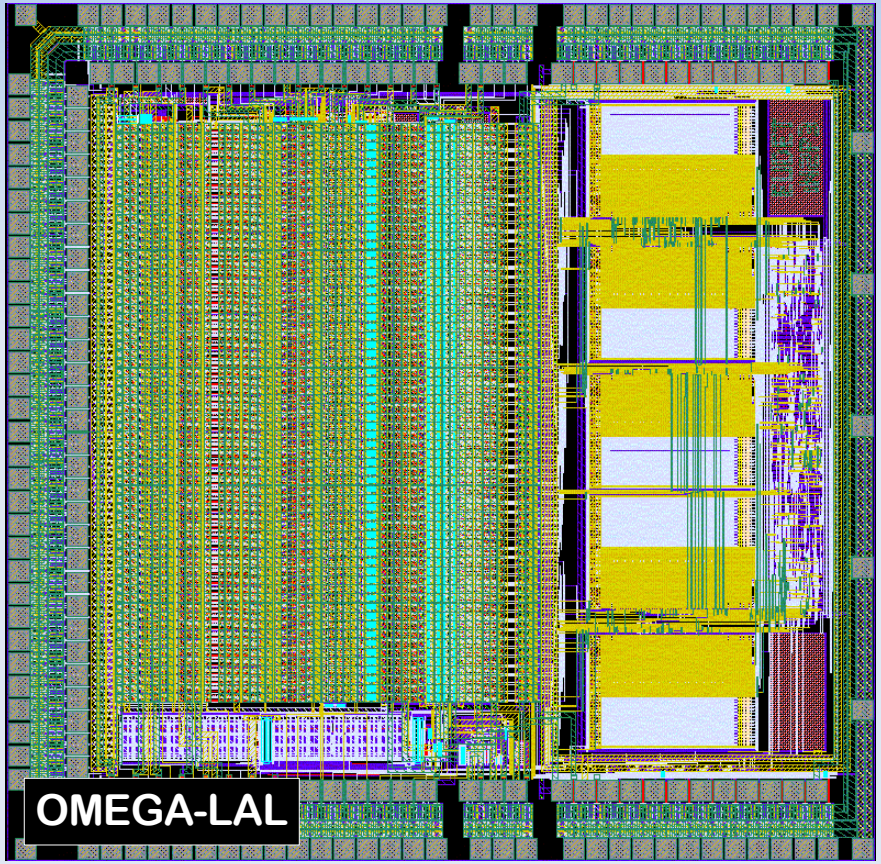


HARDROC

Prototype for 2nd gen. of ROC ASIC's (incl. local storage)
→ ECAL, AHCAL

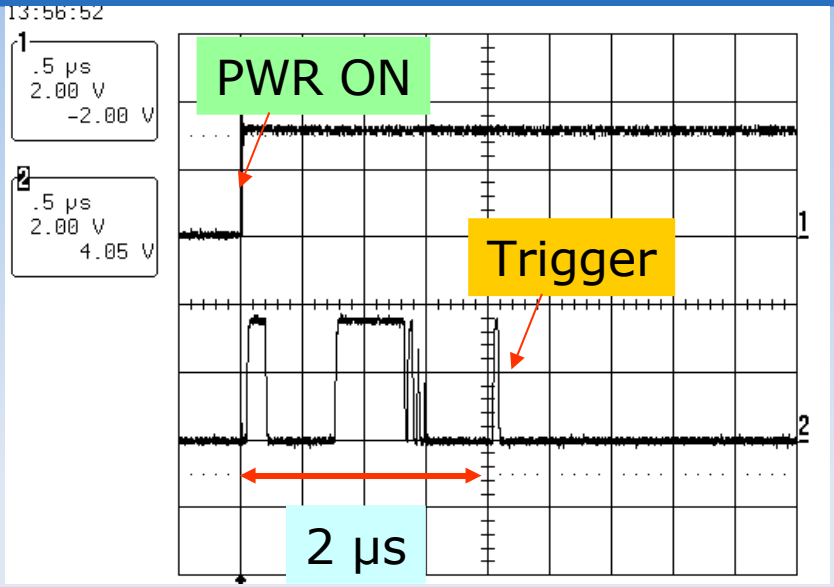
- 64 channels, 16 mm²
- Digital/analogue output.
- 2 thresholds (3 very soon)
- low consumption
  - < 10 µW/ch
  - Power pulsing
- Digital memory
  - 128 events
  - ASIC ID, BC ID, hits
- Large gain range
  - Channel wise
- X-talks < 2%
- Threshold > 10 fC
  - Adequate for GRPC*

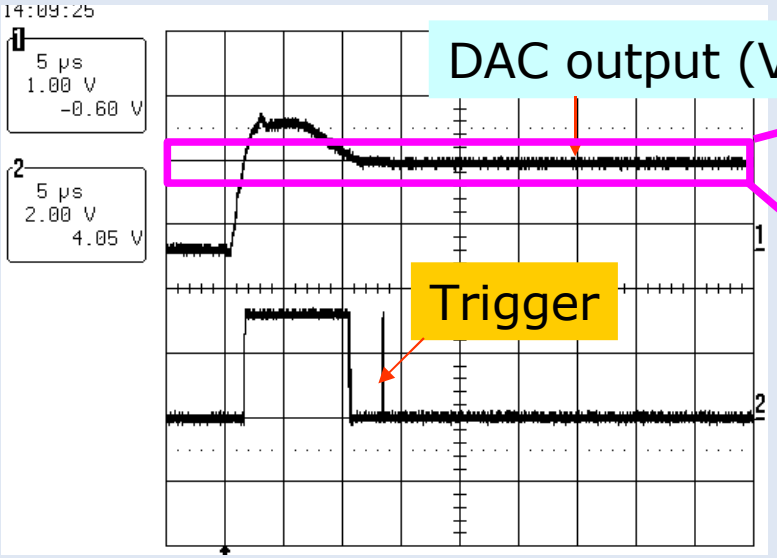
2nd gen coming soon

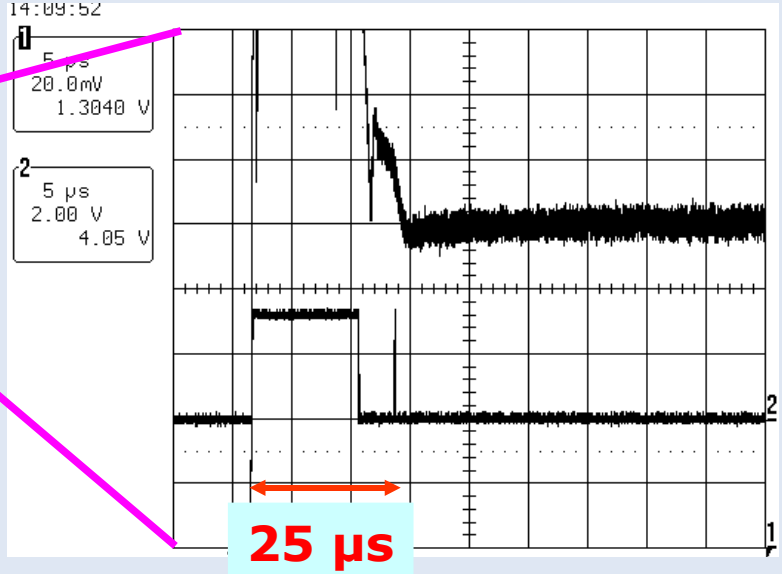


*** For µMEGAS another ASIC is developed in IPNL with a threshold as low as 3 fC**

HARDROC: Power pulsing



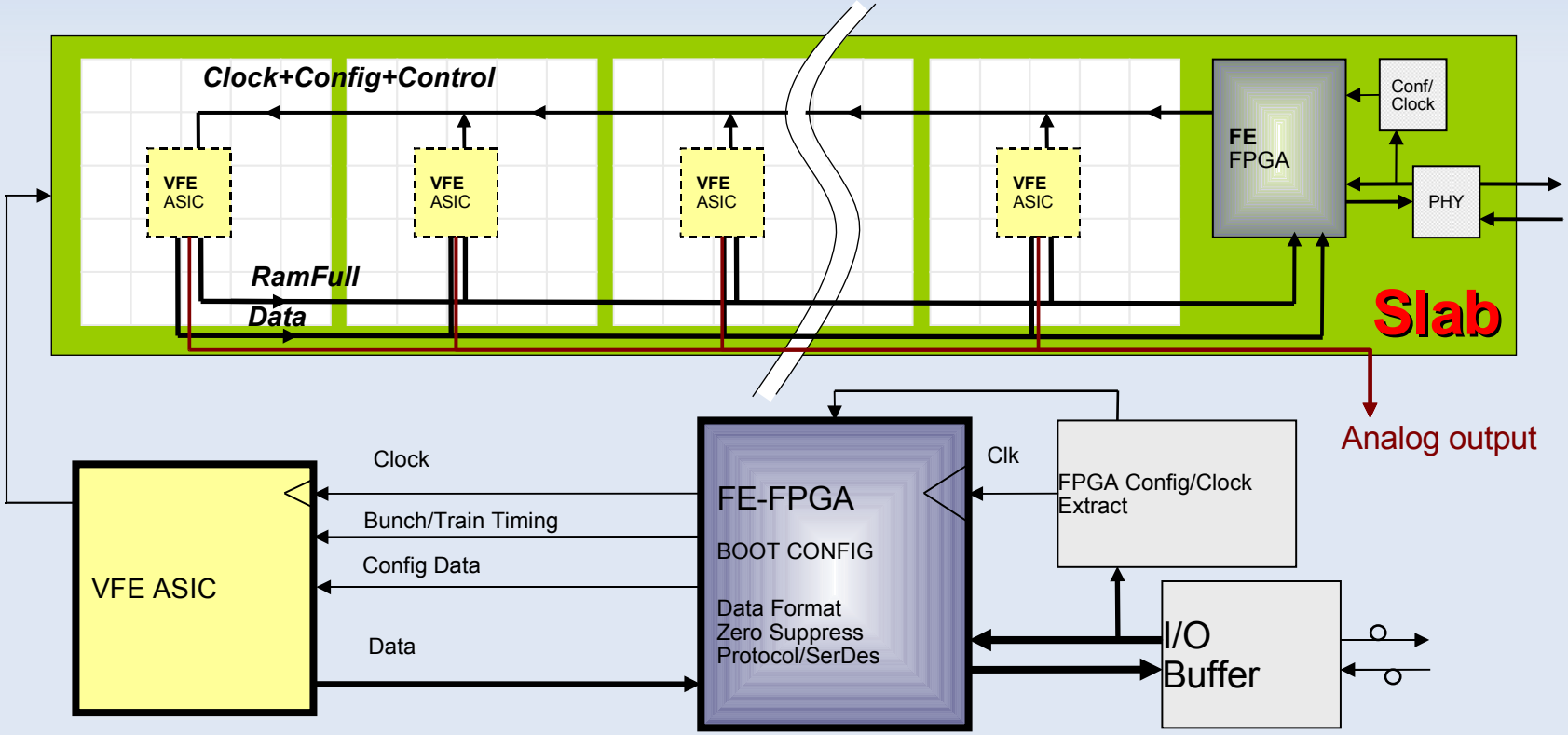




Going digital: Embedded electronics

- 1 m²
  - 10k channels
- 1 m³ (40 layers)
  - 400k channels

- Embedded Readout chips
  - 64 channels
- Daisy Chained
  - Control & readout

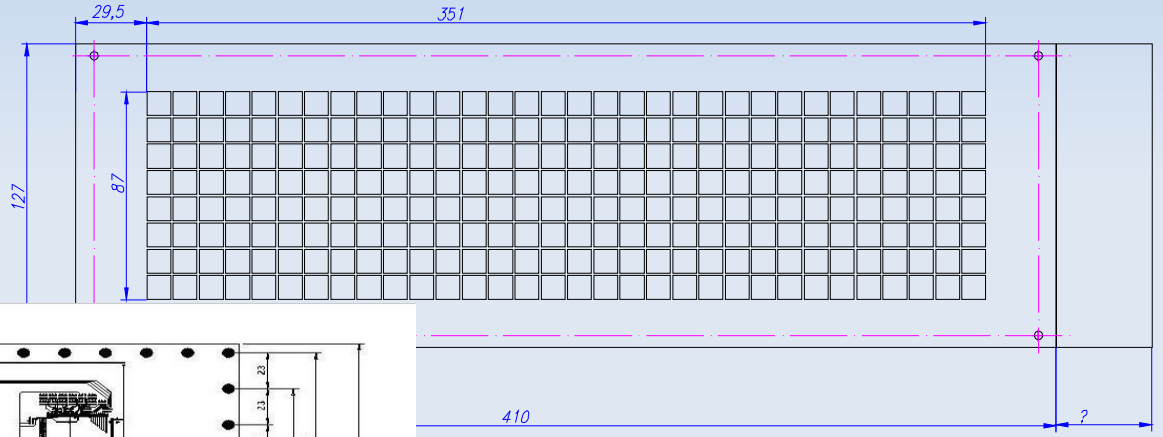


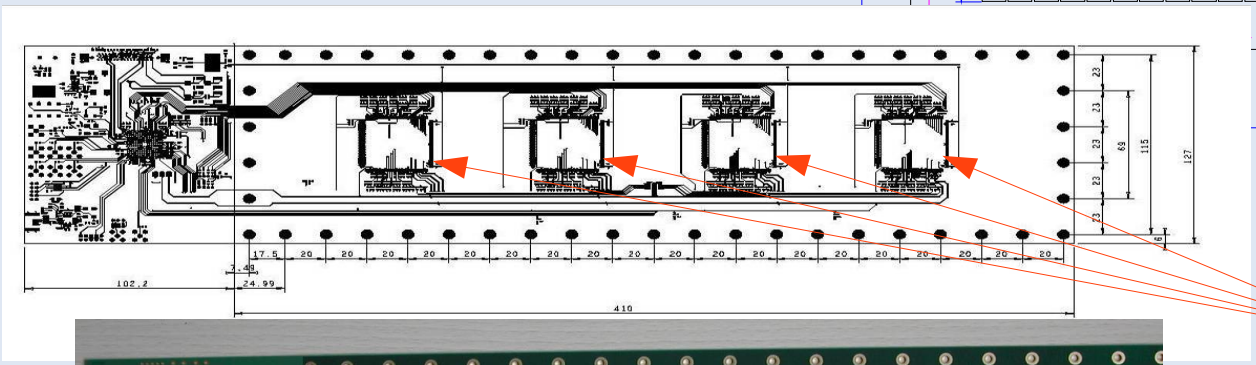
Readout system

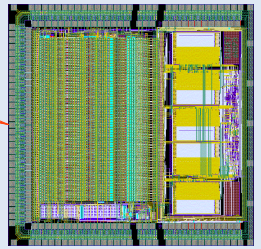
- The 4 chips are daisy-chained and connected to a FPGA communicating with a PC through a USB device.
- All components on the same PCB
- Firmware + Software (generic ROC interface library) developed **LLR**
  - Config loading
  - Acquisition modes
  - Readout & Debug
- Acquisition modes
  - Internal triggers
  - External triggers : cosmics & test beam
- Data output: The two kinds of data output of the HARDROC chips are accessible: **digital** and **analogue**

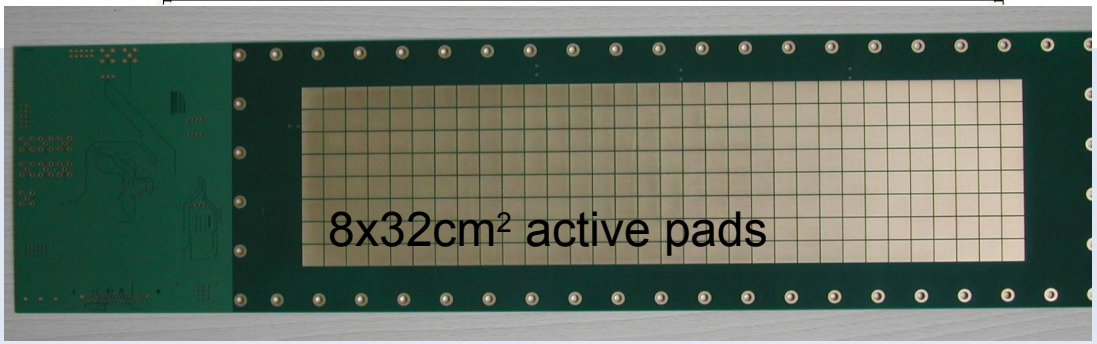
DHCAL1 test card

- 8×32 pads detector (GRPC and µMEGAS)
- 8-layer PCB
- 4 ASICs: HARDROC (Omega-LAL)
  - 64 ch
  - 2 thresholds
- Readout USB + FPGA

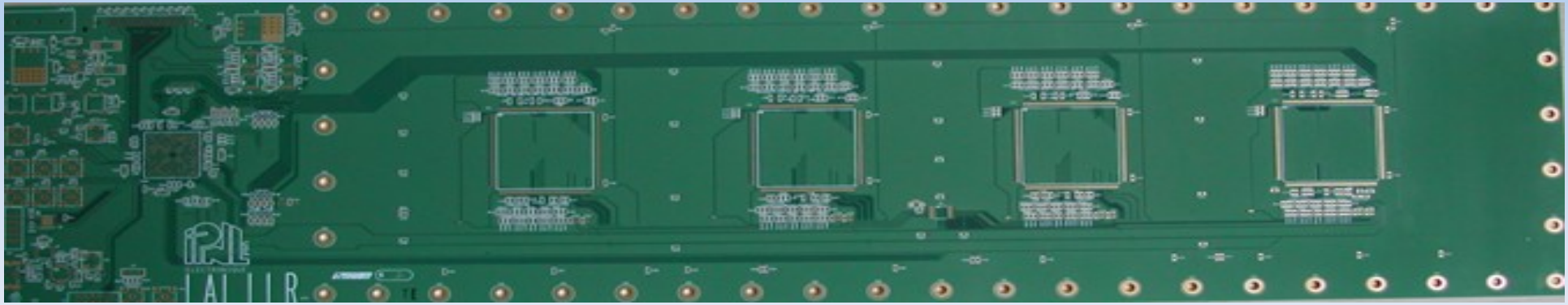


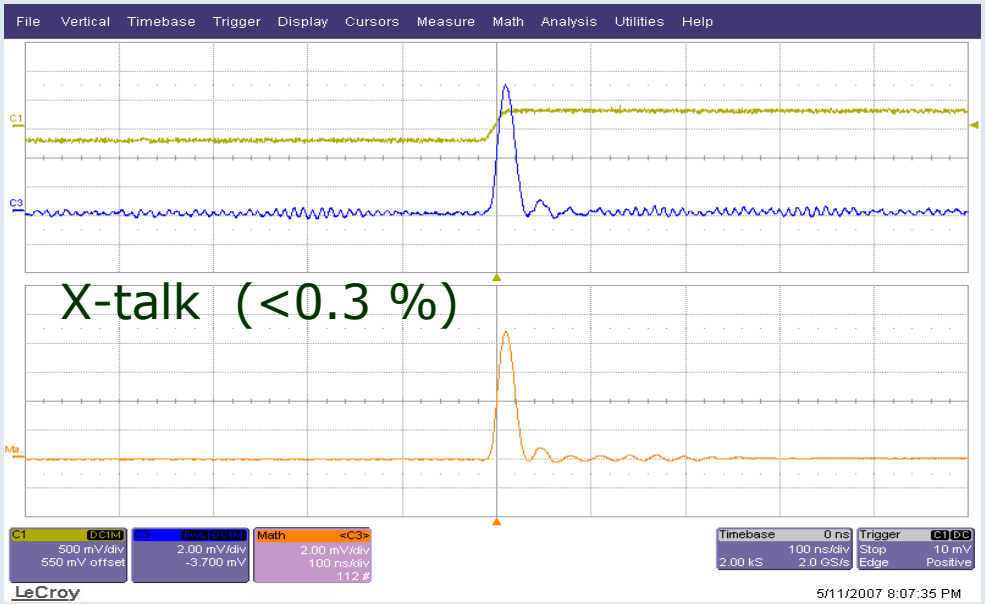


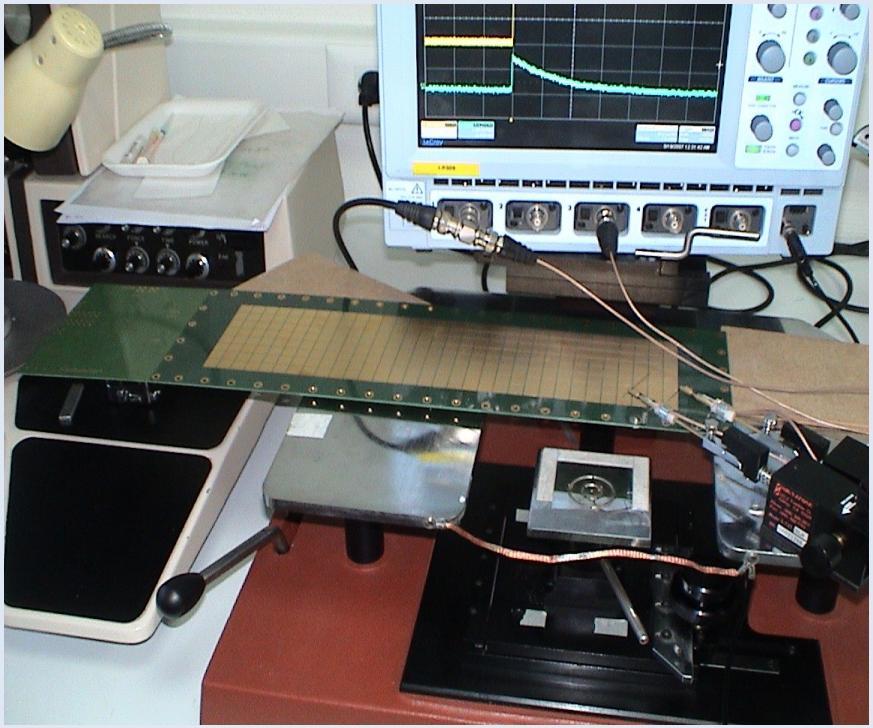


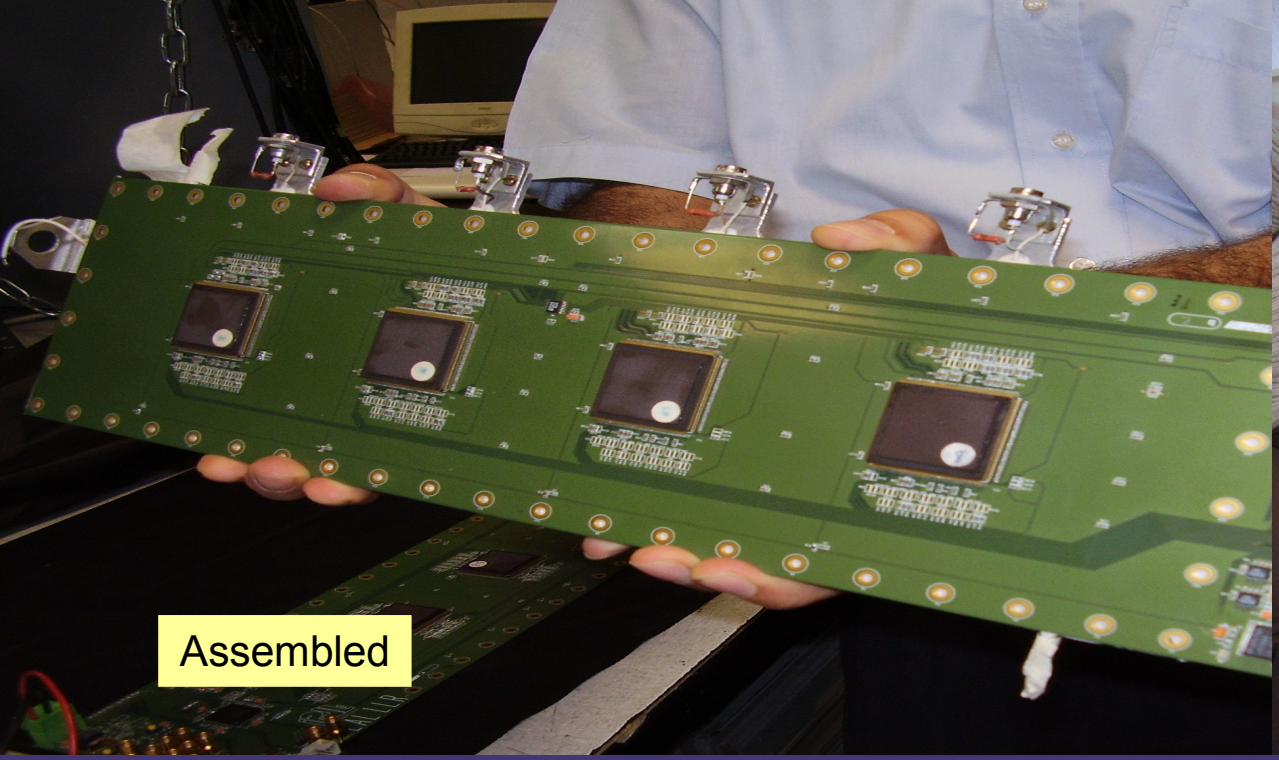


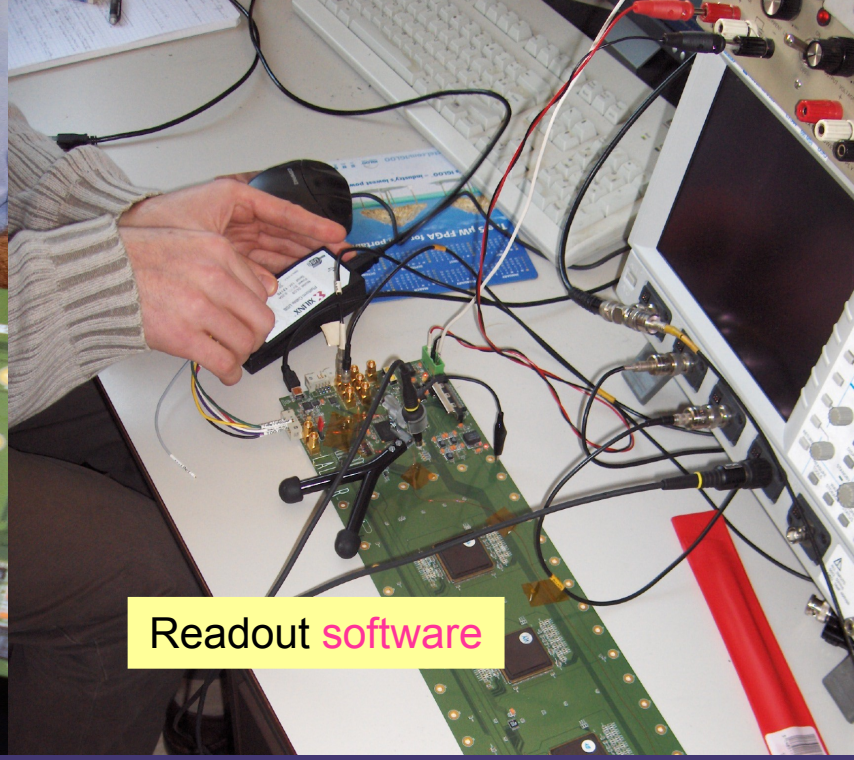
June 07:
- **8-layer PCB , 800 µm thick**
- **8×32 pads of 1 cm² and 500 µm separation**











Fichier Vertical Base de temps Déclenchement Affichage Curseurs Mesure Math Analyse Utilitaires Aide

First Daisy chain measurement

C4
C1
C2
C3

C1 DC1M	C2 DC1M	C3 DC1M	C4 DC1M
1.00 V/div	1.00 V/div	1.00 V/div	1.00 V/div
-1.010 V ofst	-1.500 V ofst	-3.560 V ofst	570 mV offset
↓ 12 mV	↓ 3.310 V	↓ 558 mV	↓ 26 mV
↑ 5 mV	↑ 536 mV	↑ 536 mV	↑ 48 mV
Δy -7 mV	Δy -2.774 V	Δy -22 mV	Δy 22 mV

Tbase	-616 µs	Déclenchem C1 DC
	200 µs/div	Normal 1.19 V
200 kS	100 MS/s	Front Positive

X1= 325.79 µs ΔX= -160.00 µs
X2= 165.79 µs 1/ΔX= -6.2500 kHz

LeCroy

Waiting for Trigger

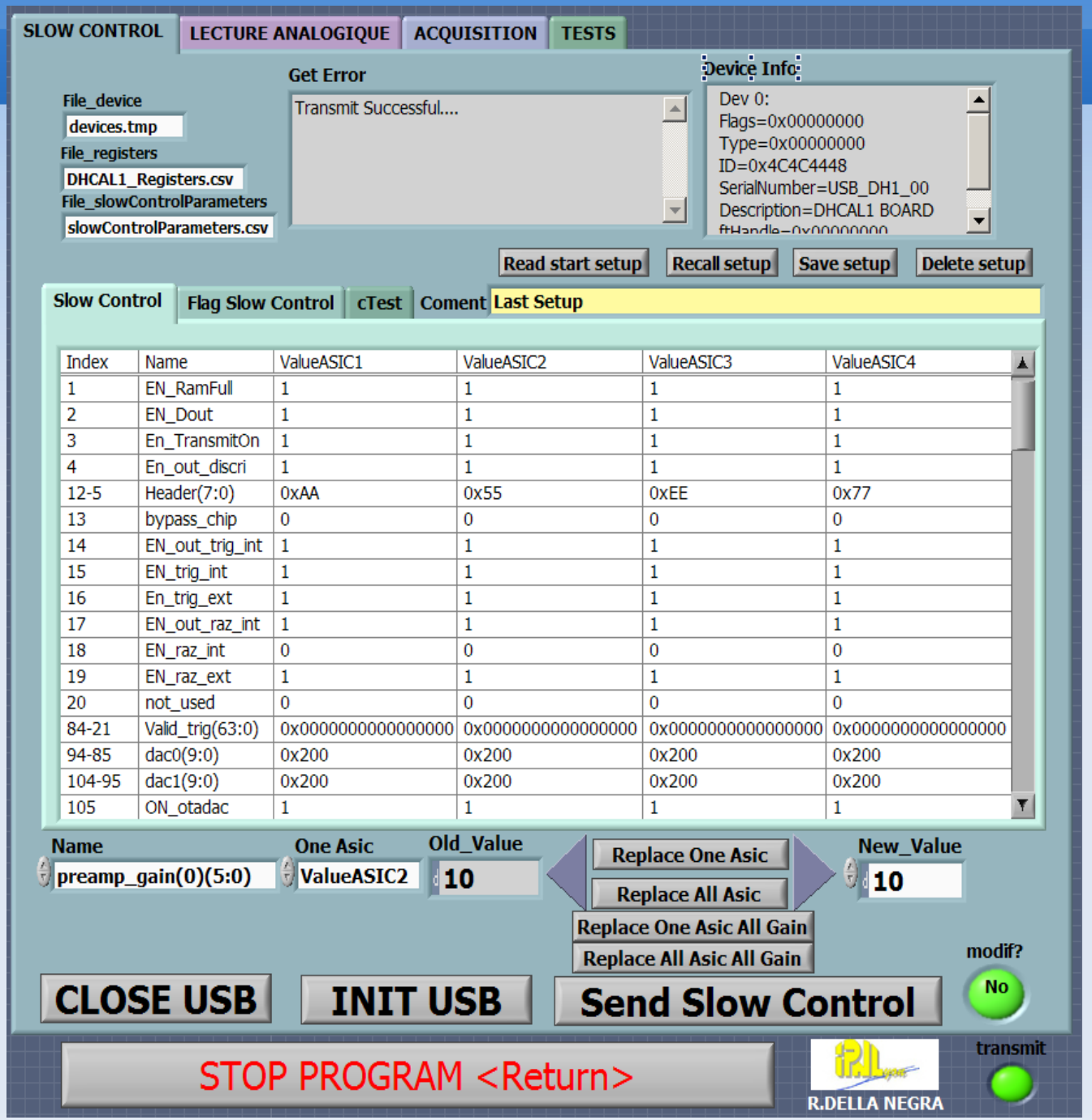
Labview DAQ

Friendly labview based system was developed

* Two thresholds

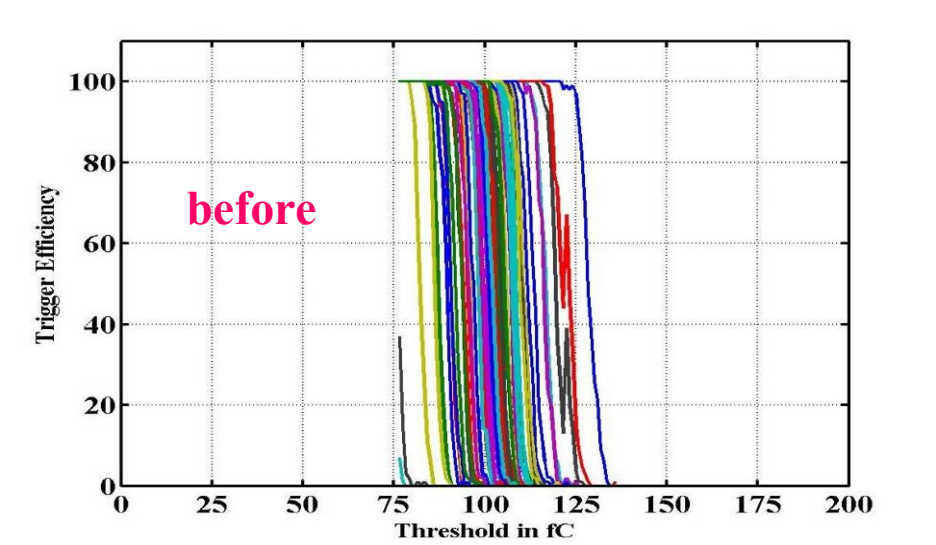
* Gain value of each channel can be Chosen in [0-63]

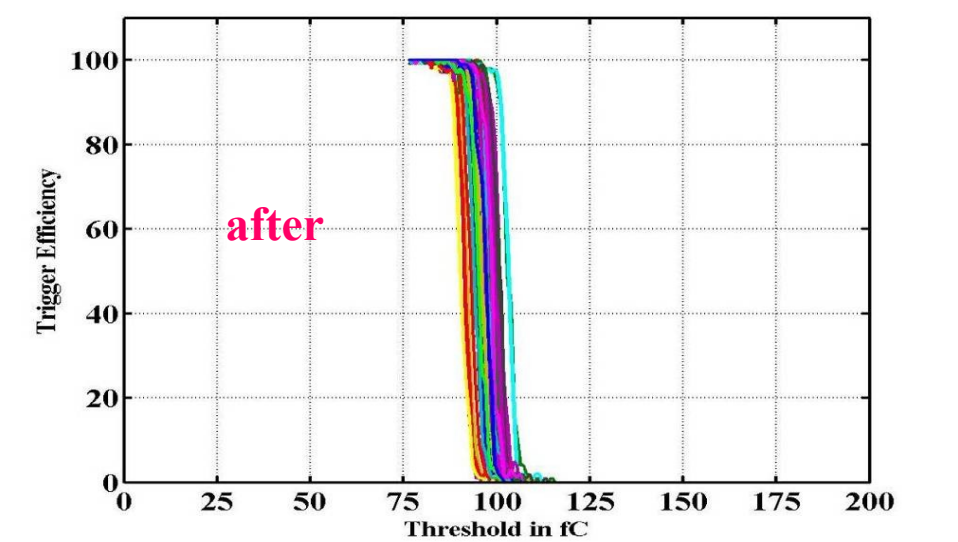
Calibration is done automatically for all channels by injecting charge through internal capacitors

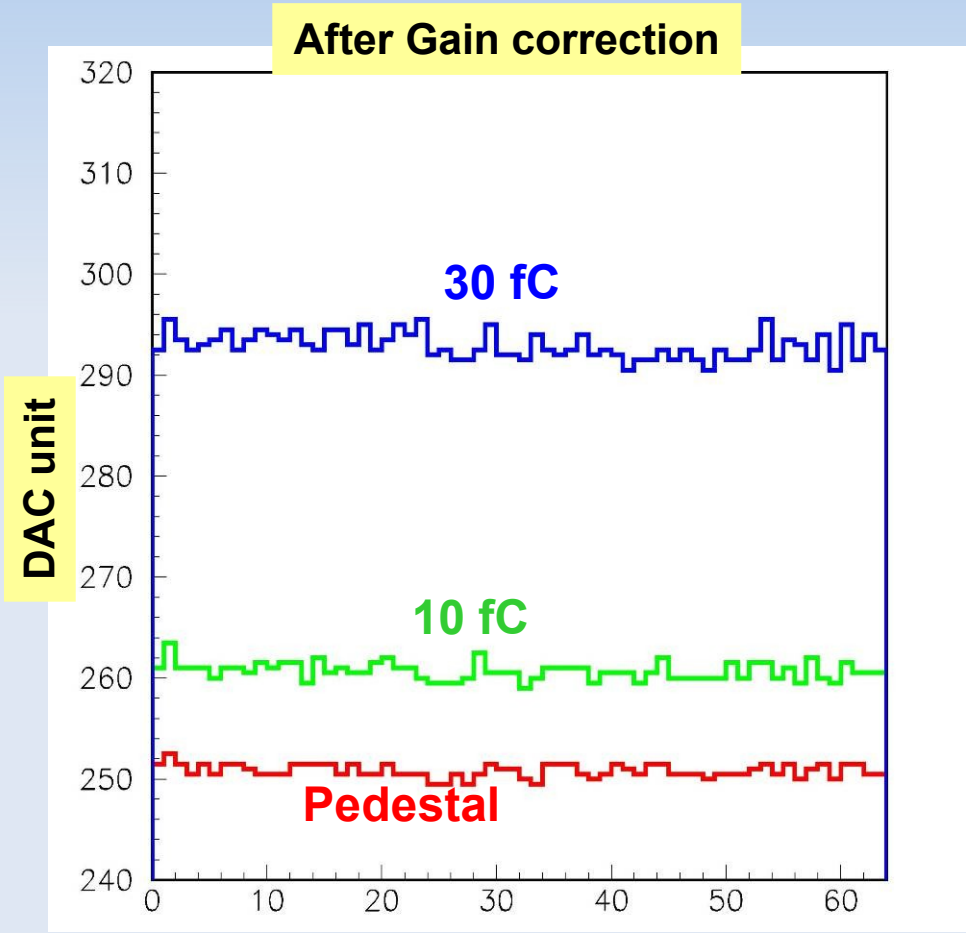


HArDROC : S-curves of 64 channels

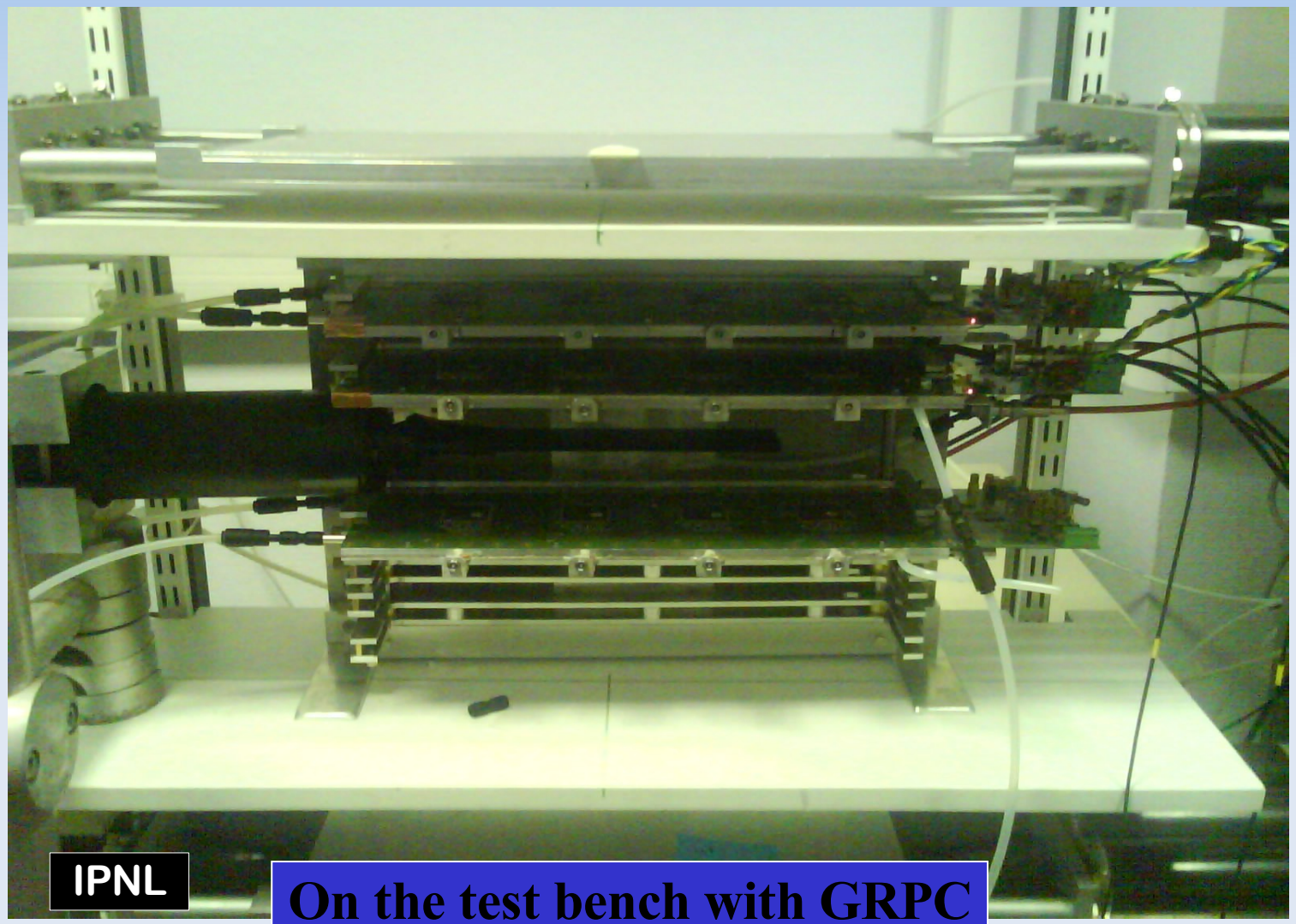
- Using on chip electronic calibration



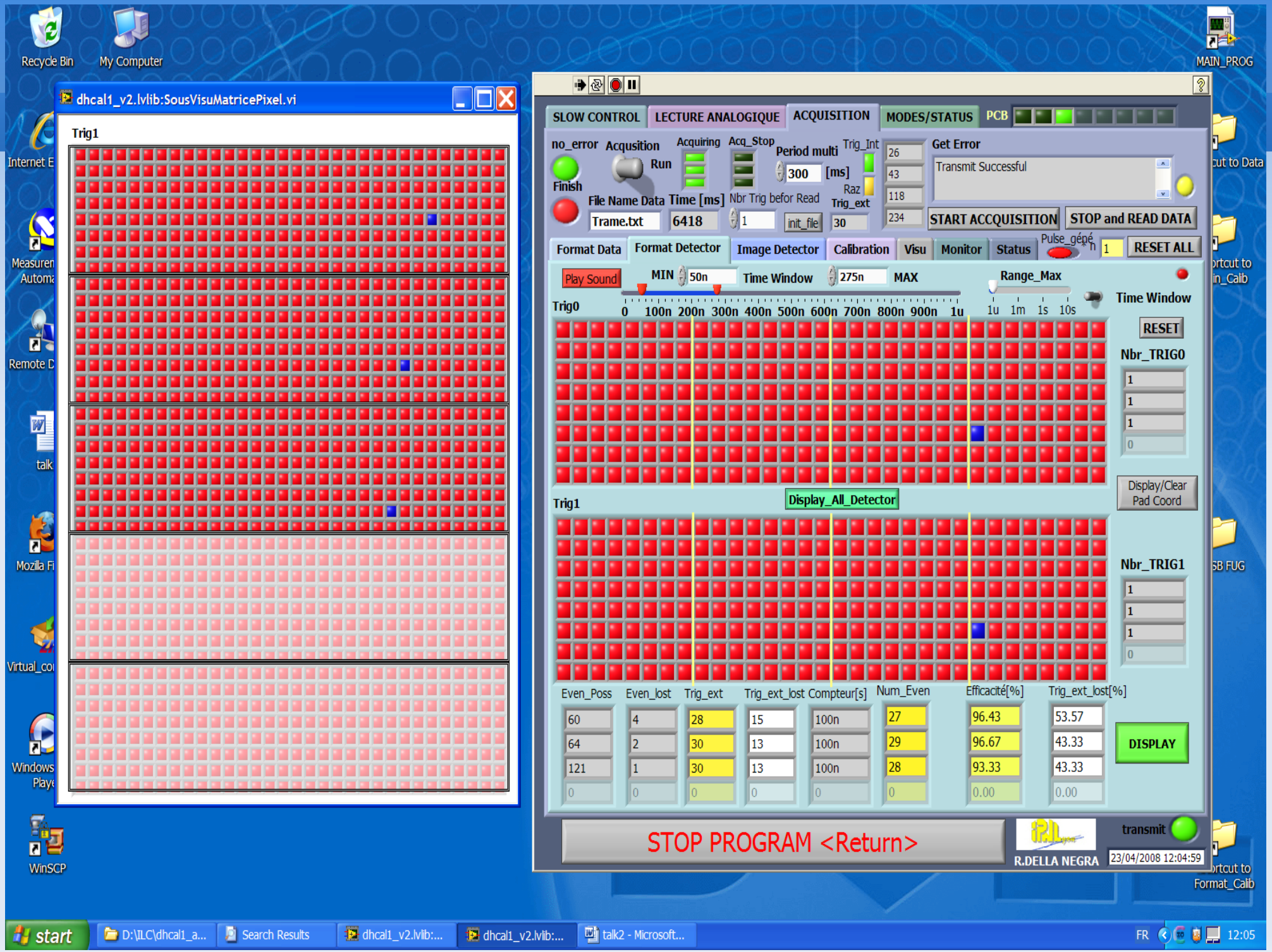




Cosmic bench

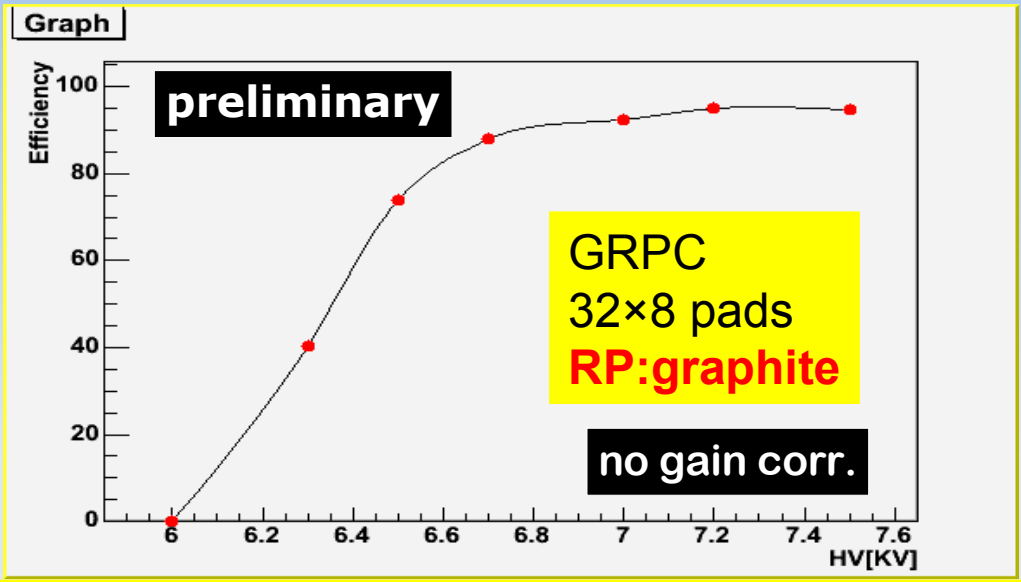


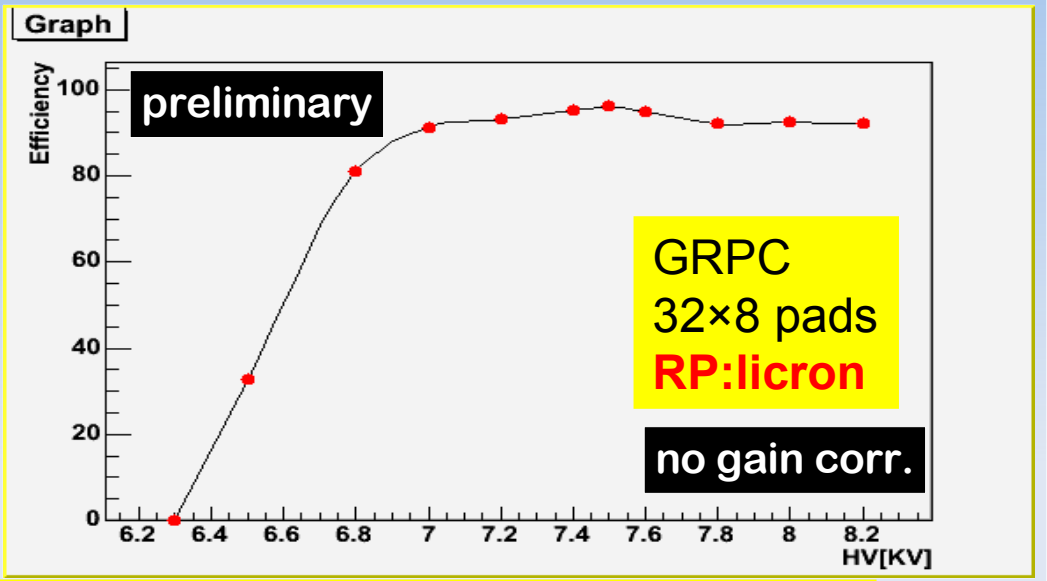
On the test bench with GRPC


dhcal1_v2.lvlib:SousVisuMatricePixel.vi
Trig1
SLOW CONTROL
LECTURE ANALOGIQUE
ACQUISITION
MODES/STATUS
PCB
no_error
Finish
Acqusition
Run
Acquiring
Acq_Stop
Period multi
300
[ms]
Trig_Int
Raz
Trig_ext
File Name Data
Trame.txt
Time [ms]
6418
Nbr Trig befor Read
1
init_file
30
26
43
118
234
Get Error
Transmit Successful
START ACCQUISITION
STOP and READ DATA
Format Data
Format Detector
Image Detector
Calibration
Visu
Monitor
Status
Pulse_généré
1
RESET ALL
Play Sound
MIN
50n
Time Window
275n
MAX
Range_Max
Trig0
0
100n
200n
300n
400n
500n
600n
700n
800n
900n
1u
1u
1m
1s
10s
Time Window
RESET
Nbr_TRIG0
1
1
1
0
Display_All_Detector
Display/Clear Pad Coord
Trig1
Nbr_TRIG1
1
1
1
0
Even_Poss
Even_lost
Trig_ext
Trig_ext_lost
Compteur[s]
Num_Even
Efficacité[%]
Trig_ext_lost[%]
60
4
28
15
100n
27
96.43
53.57
64
2
30
13
100n
29
96.67
43.33
121
1
30
13
100n
28
93.33
43.33
0
0
0
0
0
0
0.00
0.00
DISPLAY
STOP PROGRAM <Return>
R.DELLA NEGRA
transmit
23/04/2008 12:04:59
Recycle Bin
My Computer
MAIN_PROG
Internet E
Measuren Automa
Remote D
talk
Mozilla Fi
Virtual_co
Windows Playe
WinSCP
cut to Data
ortcut to in_Calib
SB FUG
ortcut to Format_Calib
start
D:\ILC\dhcal1_a...
Search Results
dhcal1_v2.lvlib:...
dhcal1_v2.lvlib:...
talk2 - Microsoft...
FR
12:05

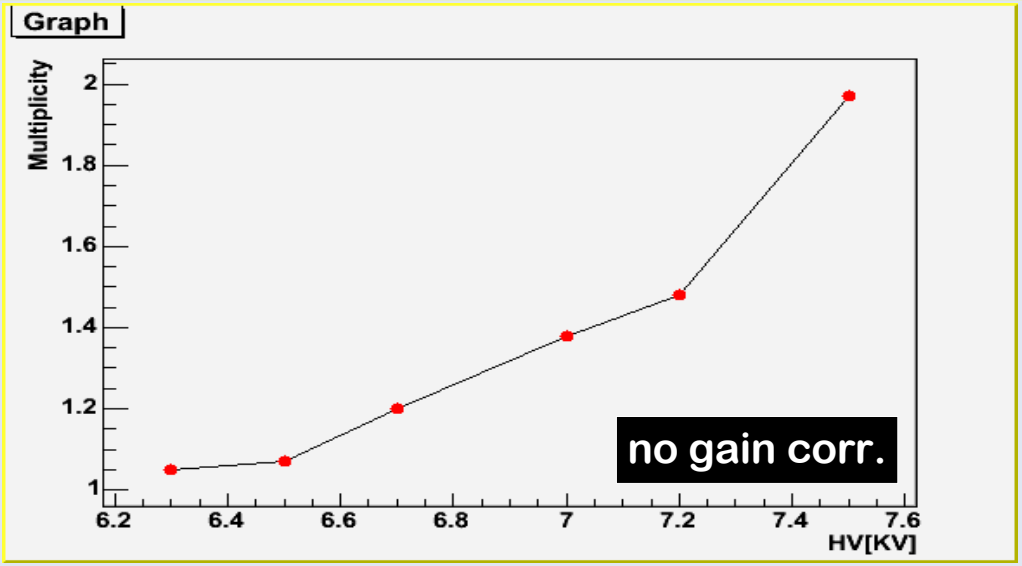
First results

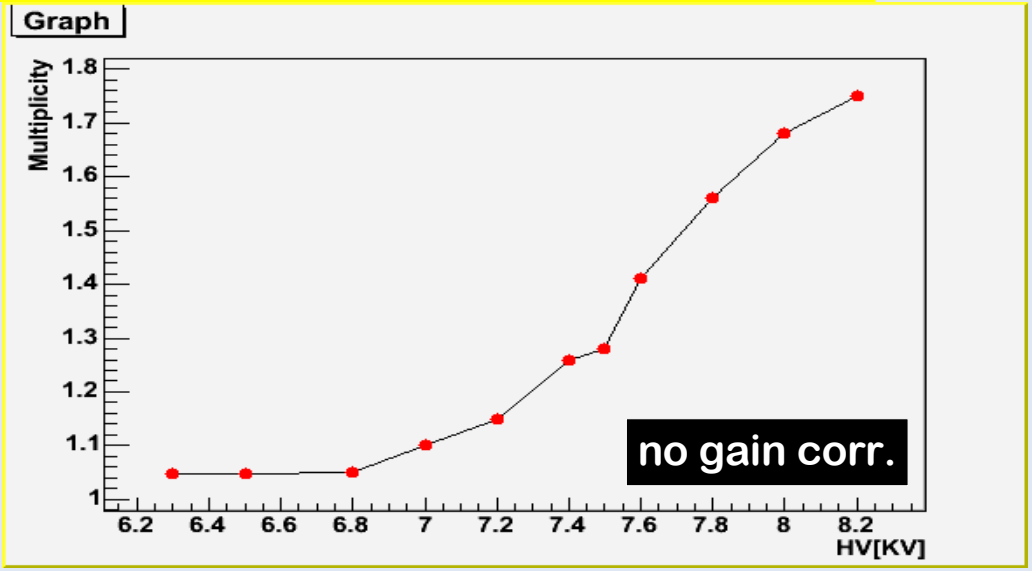
TFE	93%
Isobutene	5%
SF6	2%



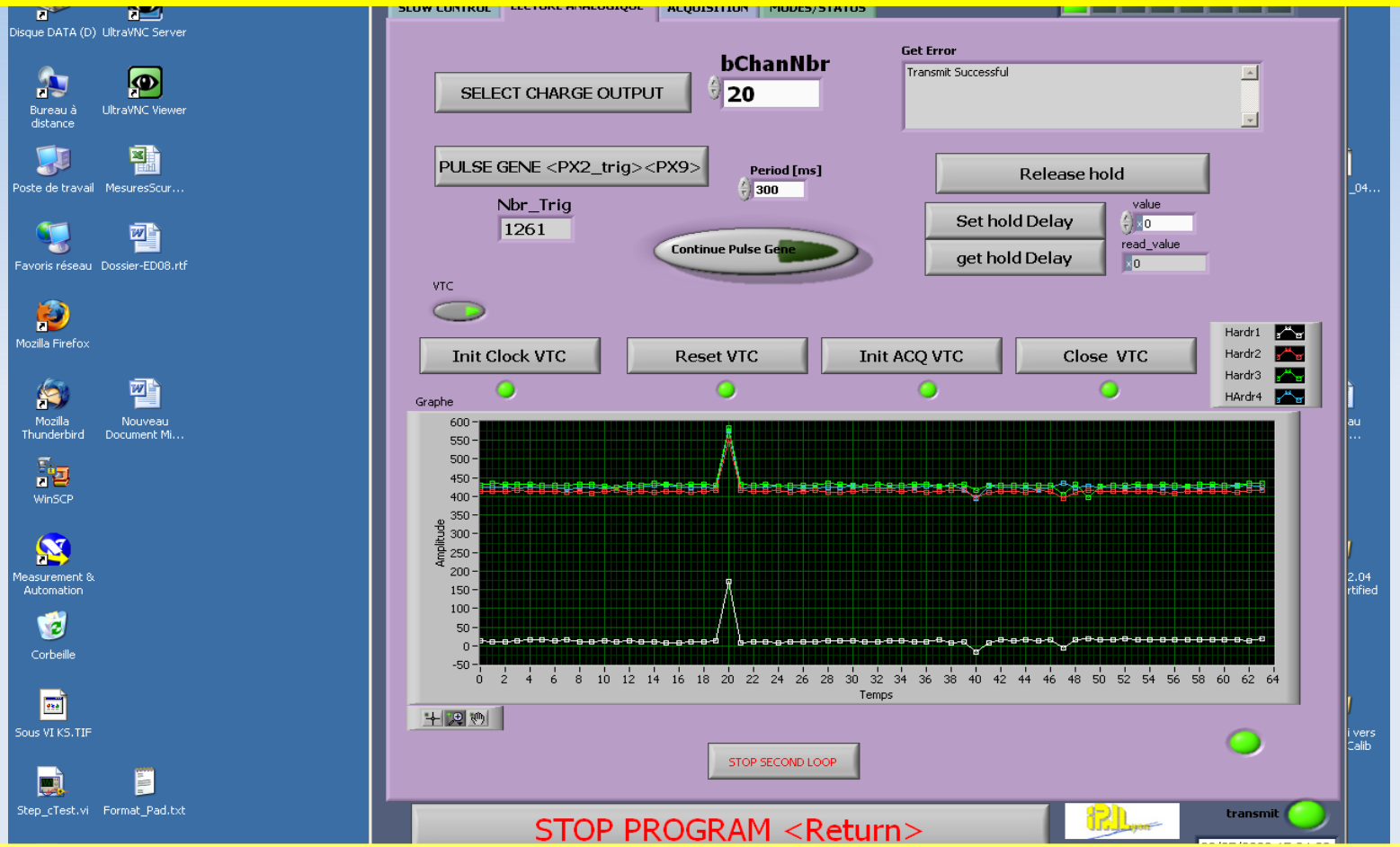


Threshold ≈ 100 fc





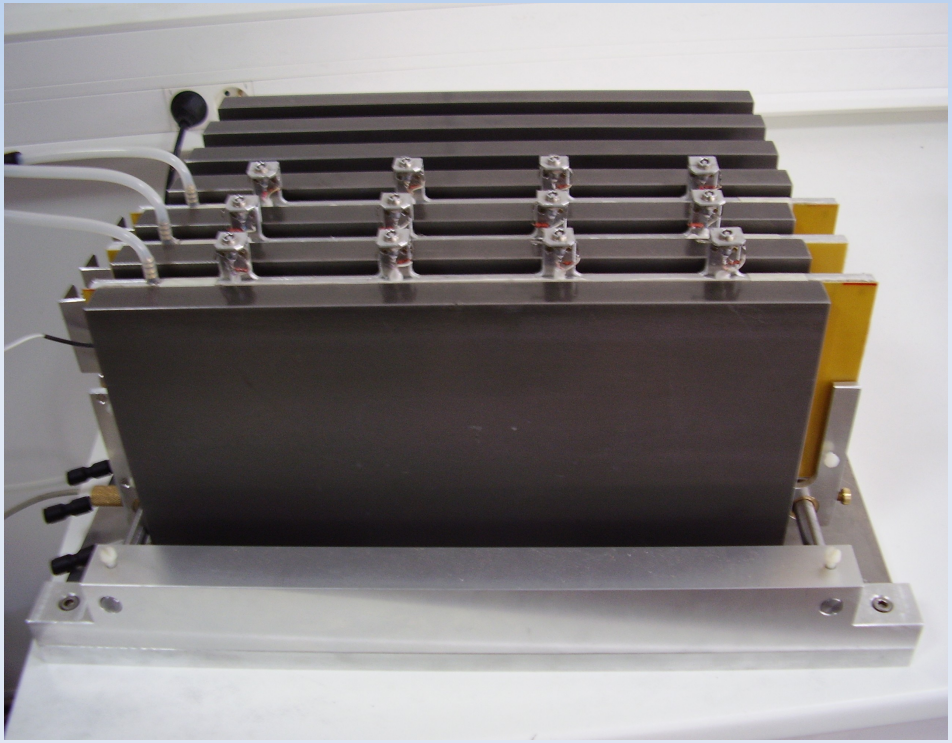
Analog readout was recently integrated and
will be used to chose the thresholds adequately



Amplitude of the signal injected in one of the 64 channels of each of the 4 ASICs through internal capacitors

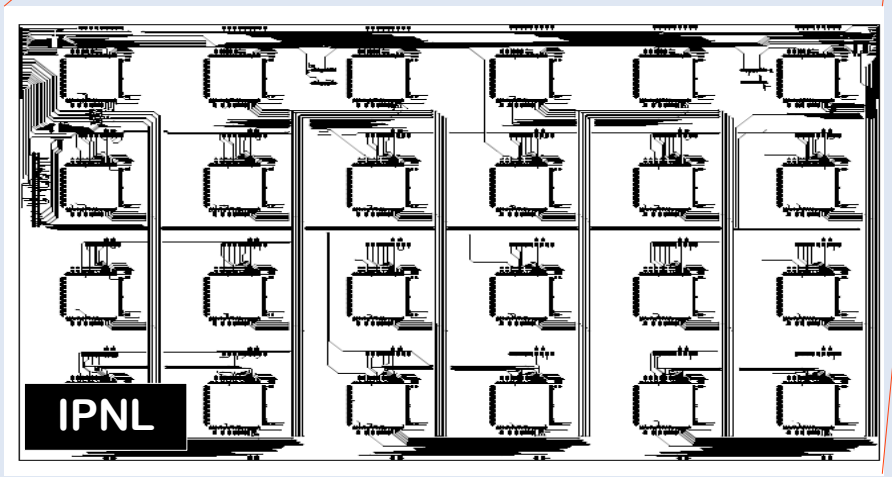
Beam tests

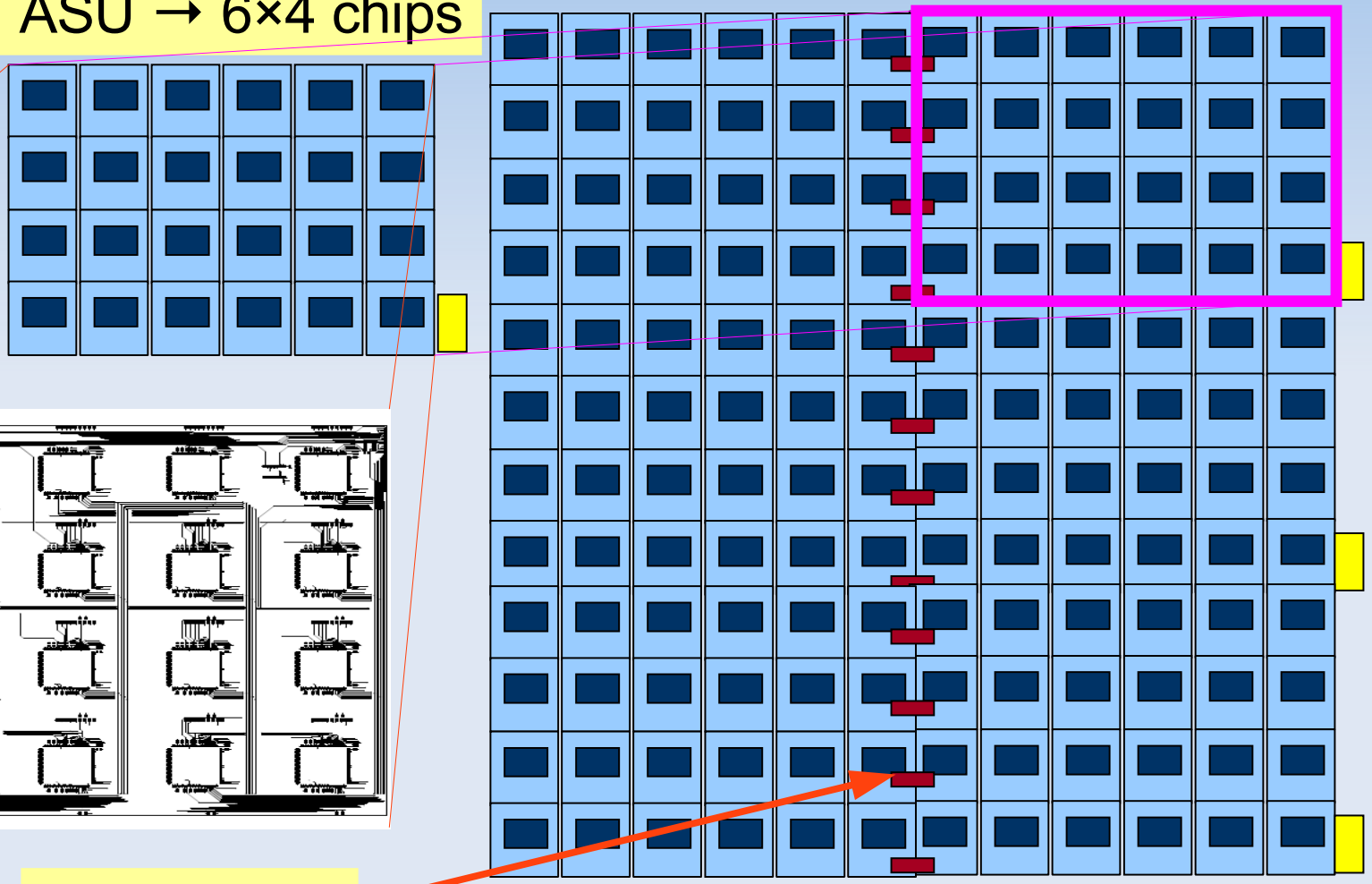
- 5 fully equipped detectors (32×8 pads each): **GRPC & µMEGAS**
- 10-17 July : CERN PS
  - µ, low energy π's
- 3-11 August : CERN SPS
  - higher energy µ, π, e's
- Program:
  - Efficiency and multiplicity
    - vs: angle, position, particle multiplicity
  - but also the first phase of the Hadronic shower



Next steps: m²
ASIC support Units

1 ASU → 6×4 chips

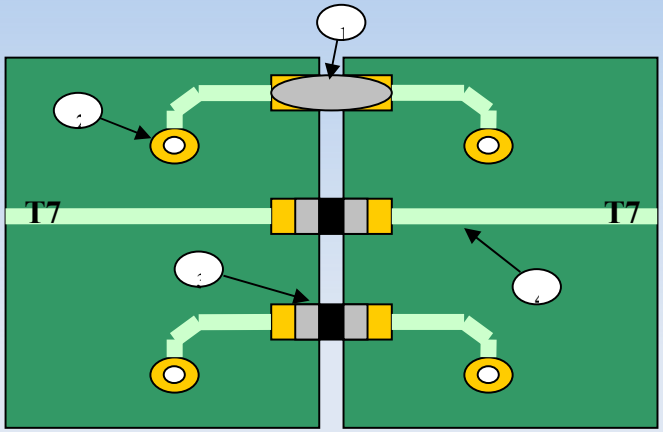


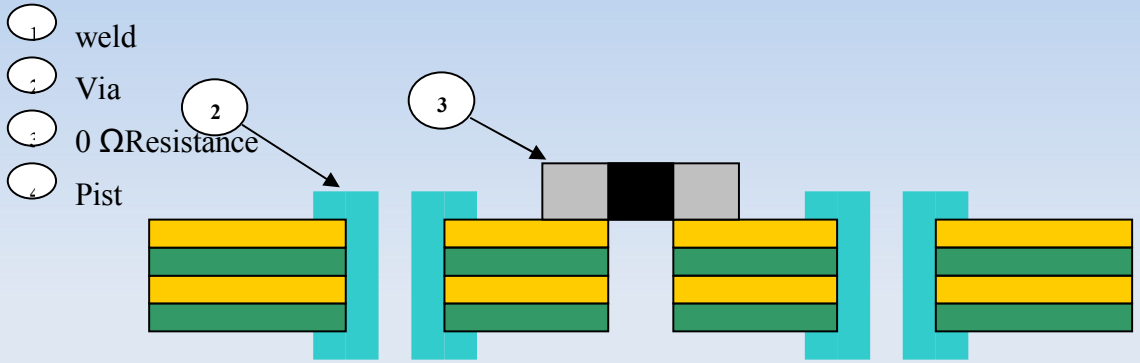


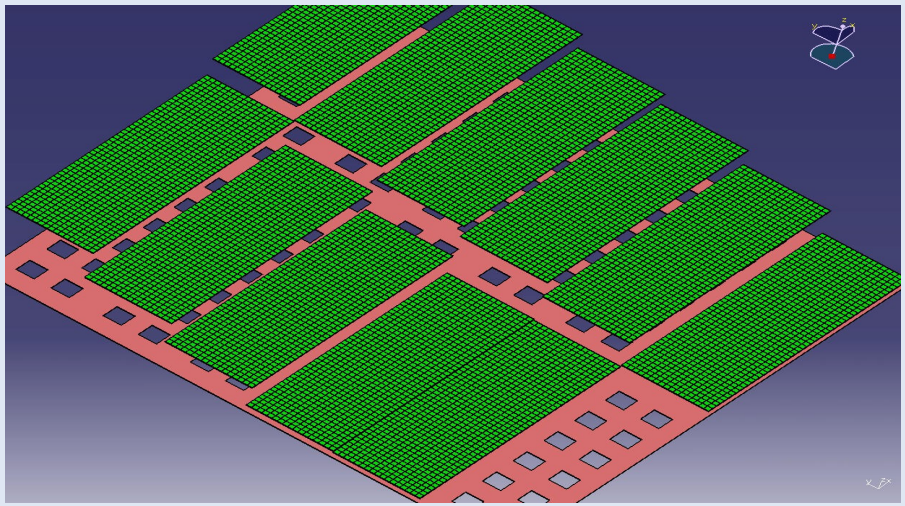
pcb-connector

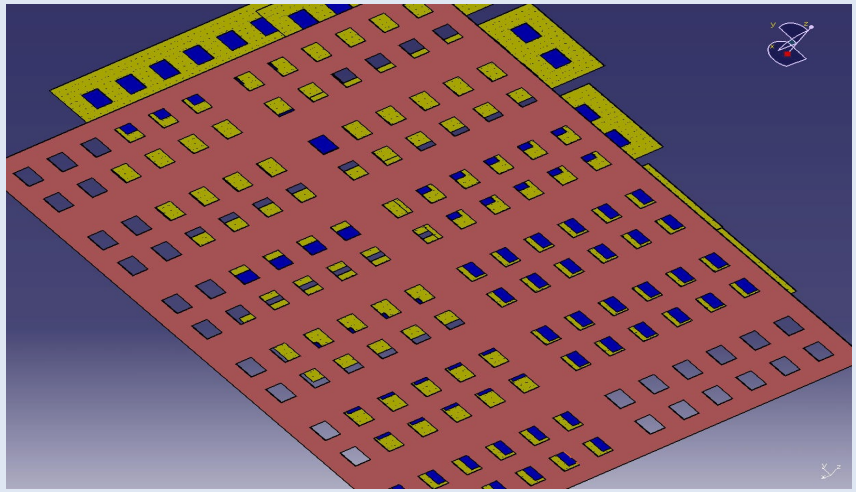
ASU hosting 24 HARDROC chips designed

Connection between the different ASU is under study: signal transmission+ mechanics (IPNL+CIEMAT)

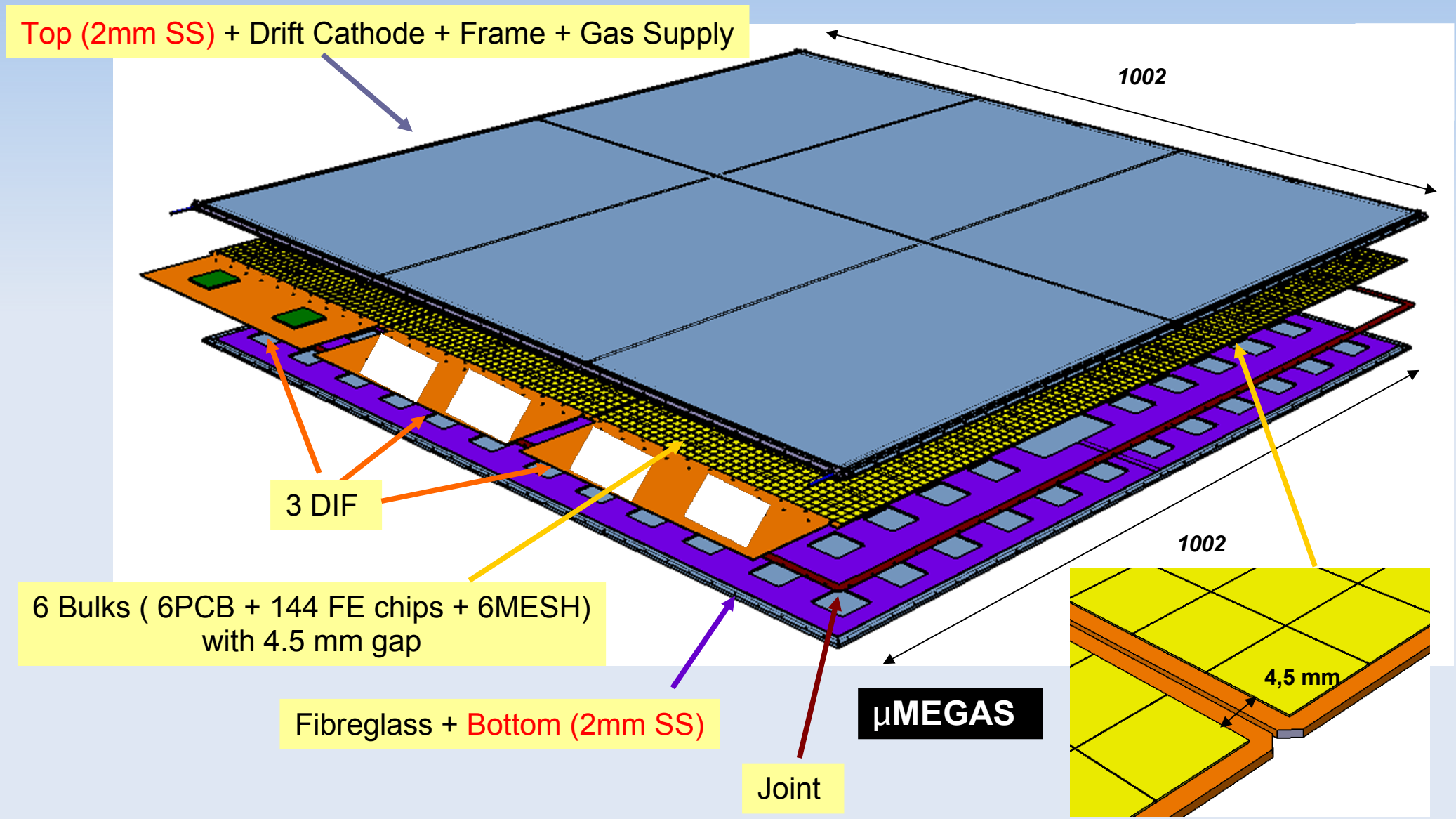




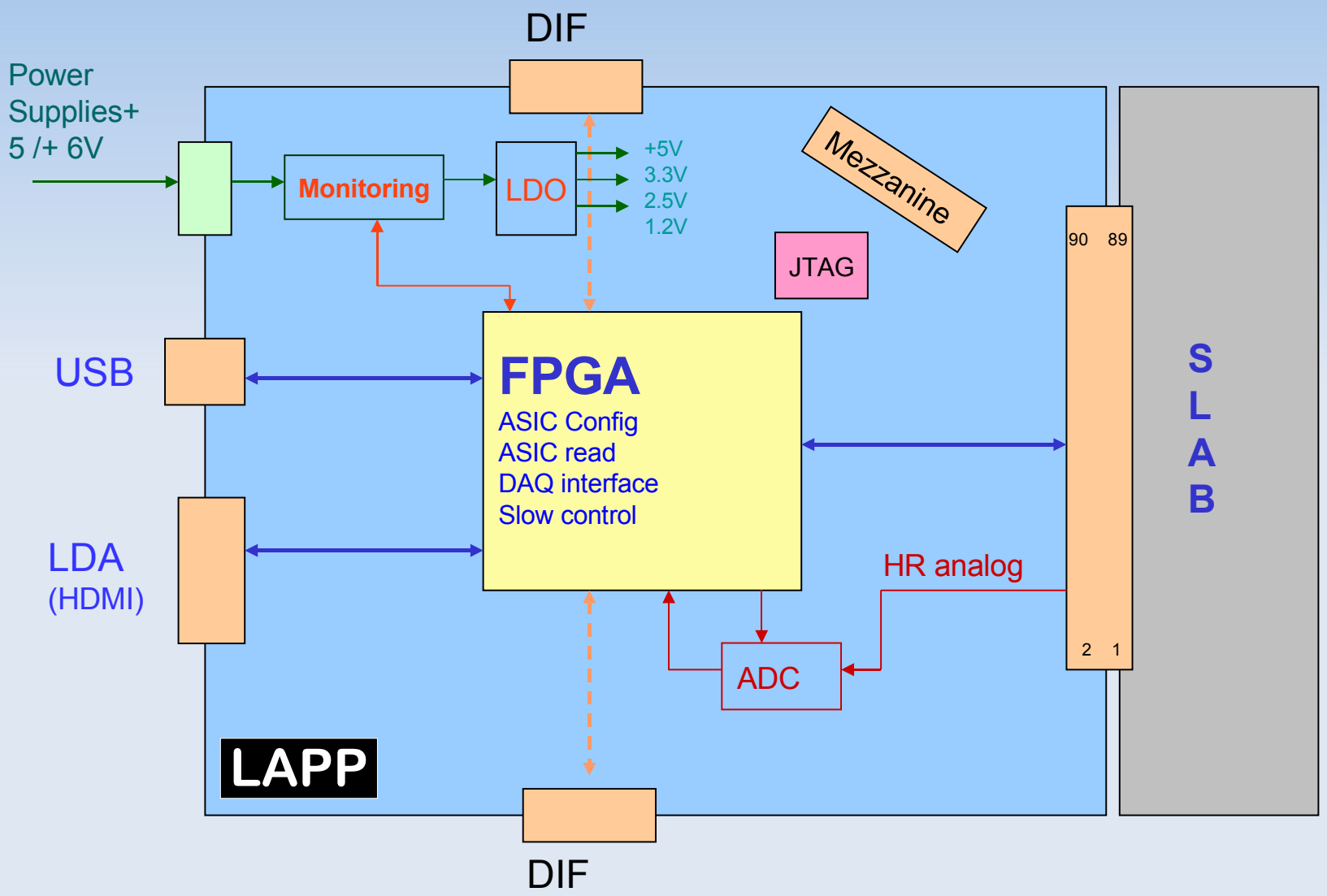




Mechanical design of a 1 m² prototype

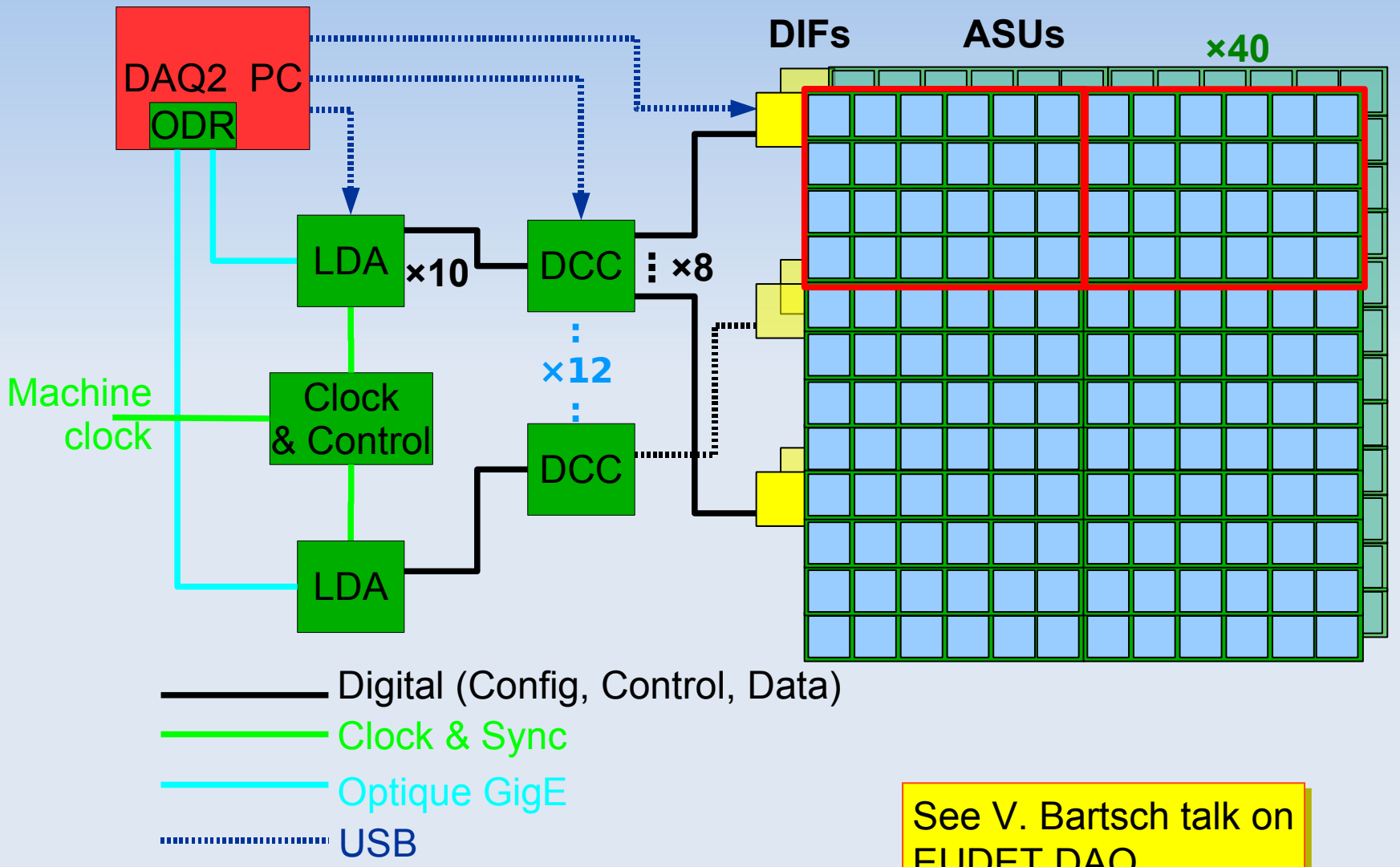


Detector InterFace card



DIF designed and sent to fabrication

First test of EUDET DAQ2

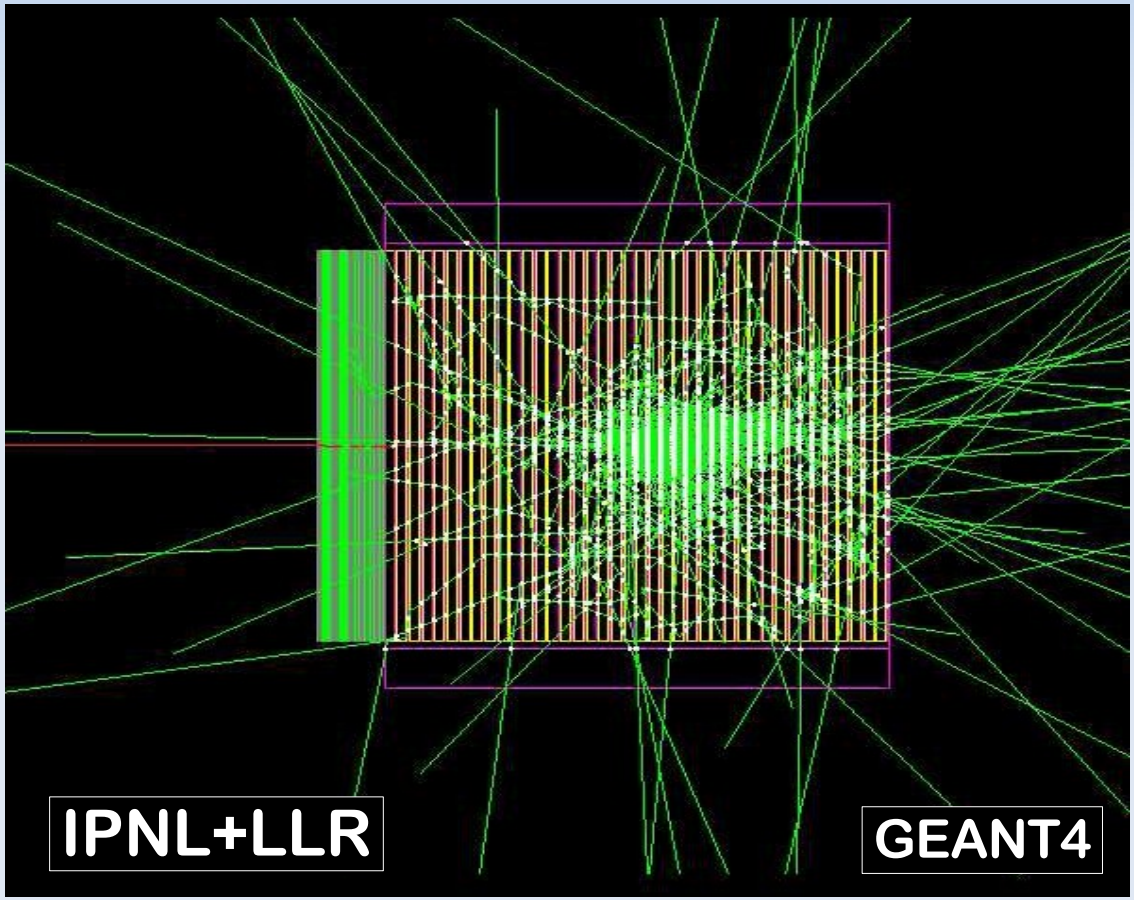


See V. Bartsch talk on EUDET DAQ

Next step: m³

Perspectives

A 1 m³ technological prototype ILC-Module0
to be built before 2010



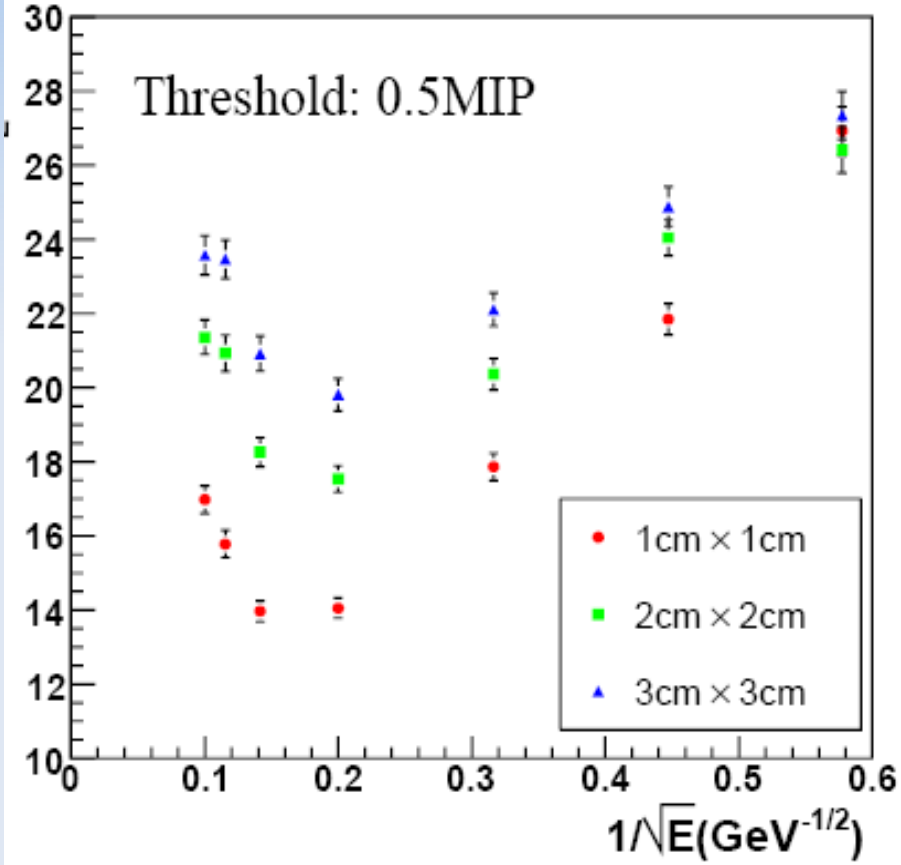
The technological prototype design optimization on going

Conclusions & perpectives

- A **D**igital **HA**dronic **CAL**orimeter with **semi-digital** (2-3 thr.) readout is very promising candidate for future collider experiments
  - integration work going on ⇒ see ILD & SiD pres.
- Small & big GRPC & µMEGAS detectors **realised and tested**
- A multi-slice test based on the **embedded** semi-digital readout was successfully tested in a laboratory cosmic bench
- A **beam test** is scheduled next month at CERN.
- **1 m² project** is ongoing and the first plane is expected before the **end of 2008**.
- A full **1 m³ technological prototype** is funded and expected in **2009-2010**

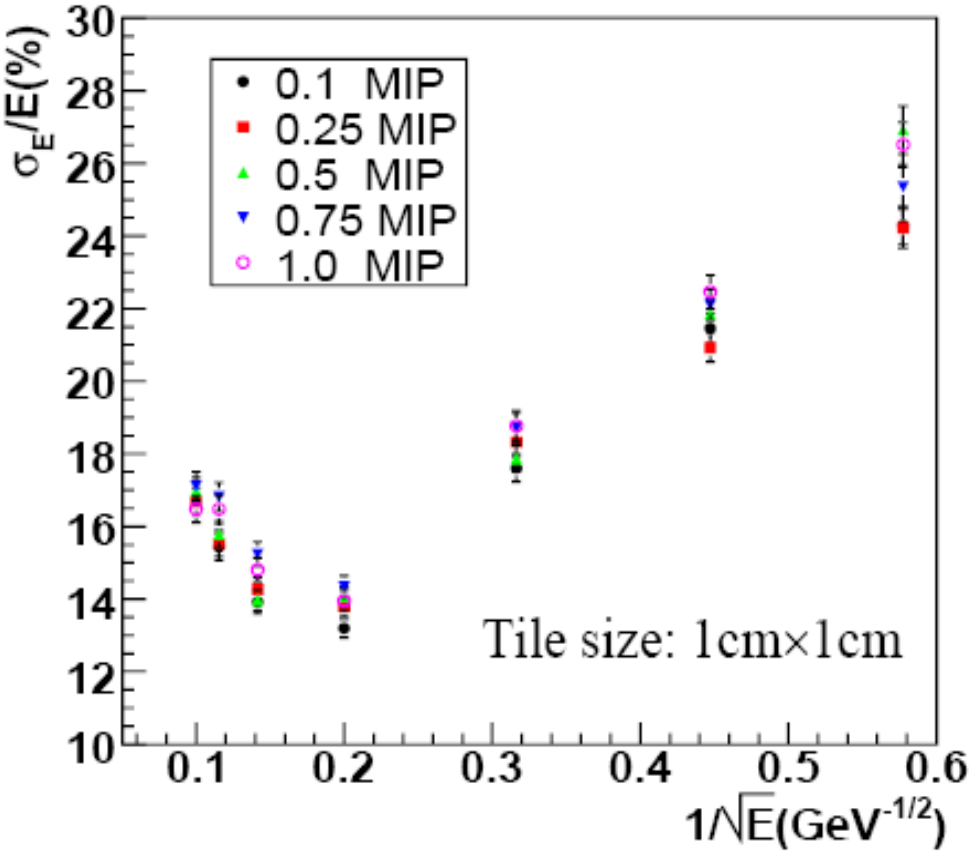
Energy Resolution

Segmentation dependence



→ Smaller size is better in high energy region

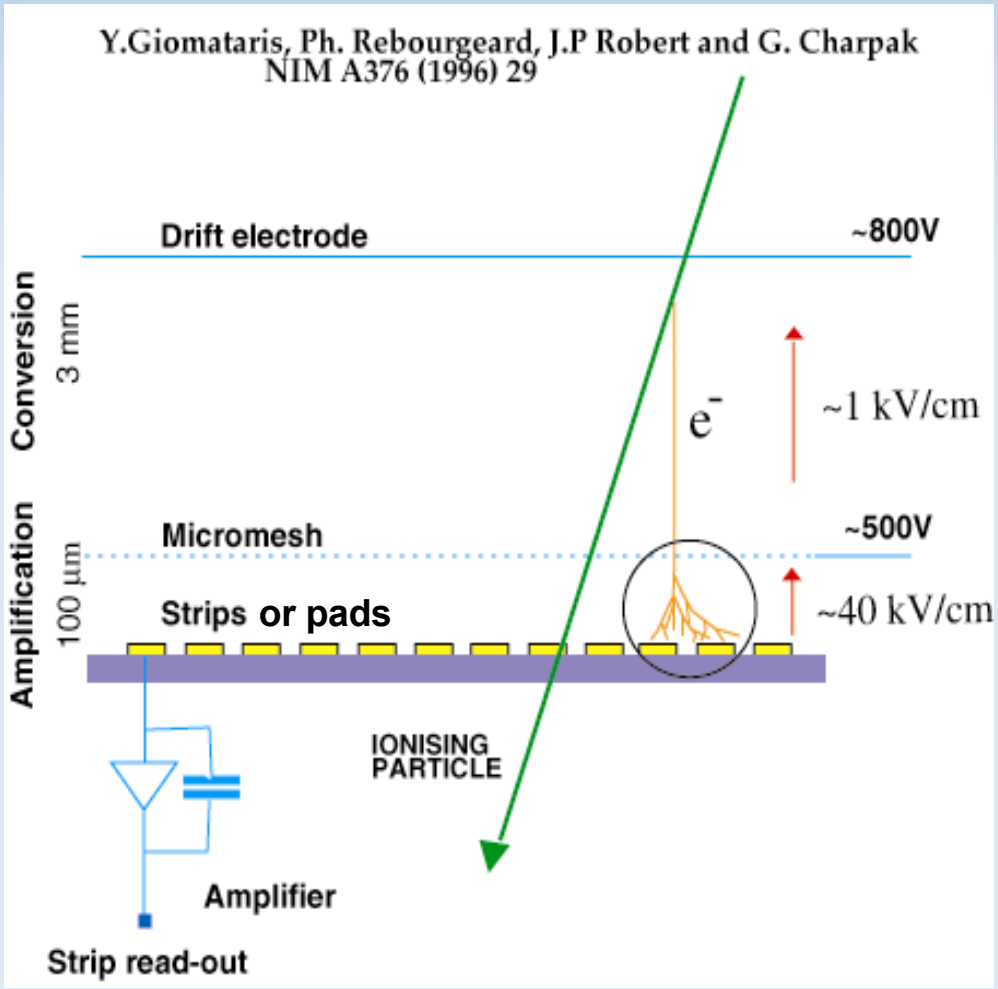
Threshold dependence

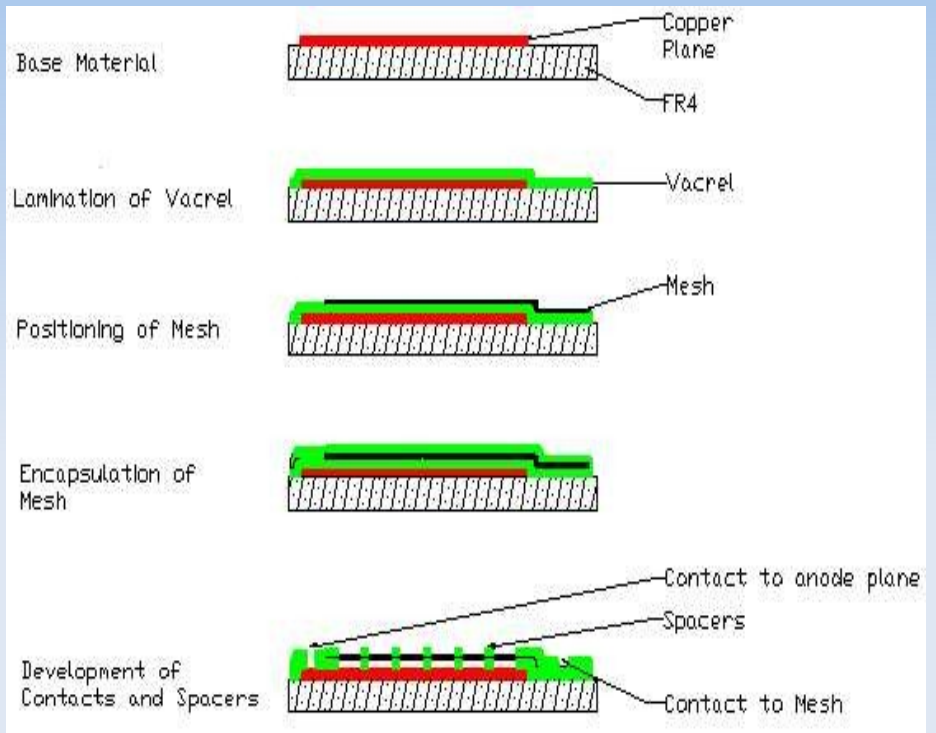


→ No significant difference

Micro Mesh gaseous structure

- The bulk technology





mesh + PCB = 1 block: the bulk

robustness

large area

uniformity

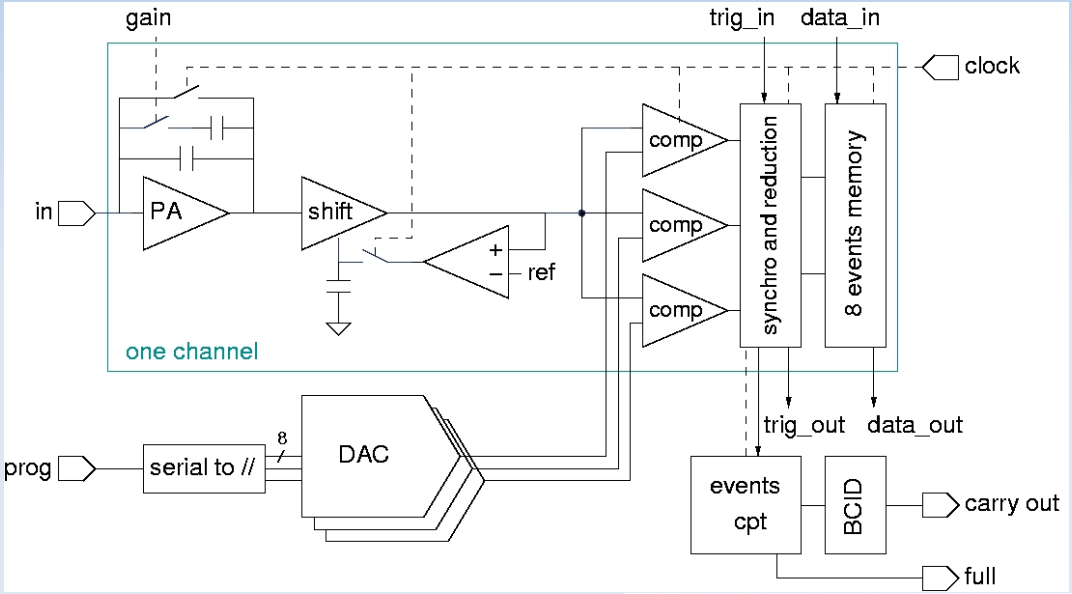
industrial process…

MicroMegas Prototypes

- PCB and bulk from CERN (*Rui de Oliveira*)
  - 325 LPI mesh
  - spacers : 120 µm height
    300 µm diameter
  - pads : 0.98×0.98 cm^2, 200 µm between pads
- The chamber
  - 95% Argon, 5% Isobutane
  - conversion volume (3mm)
  - a top in Stainless Steel with a copper drift cathode
- The pad readout : analogue
  - Gassiplex board : 6 gassiplex chips - 96 channels
    Electronics card built for CAST by DAPNIA (P. Colas, Philippe Abbon)
  - VME sequencer and ADC from CAEN
  - CENTAURE acquisition (SUBATECH, Nantes, D.Roy)

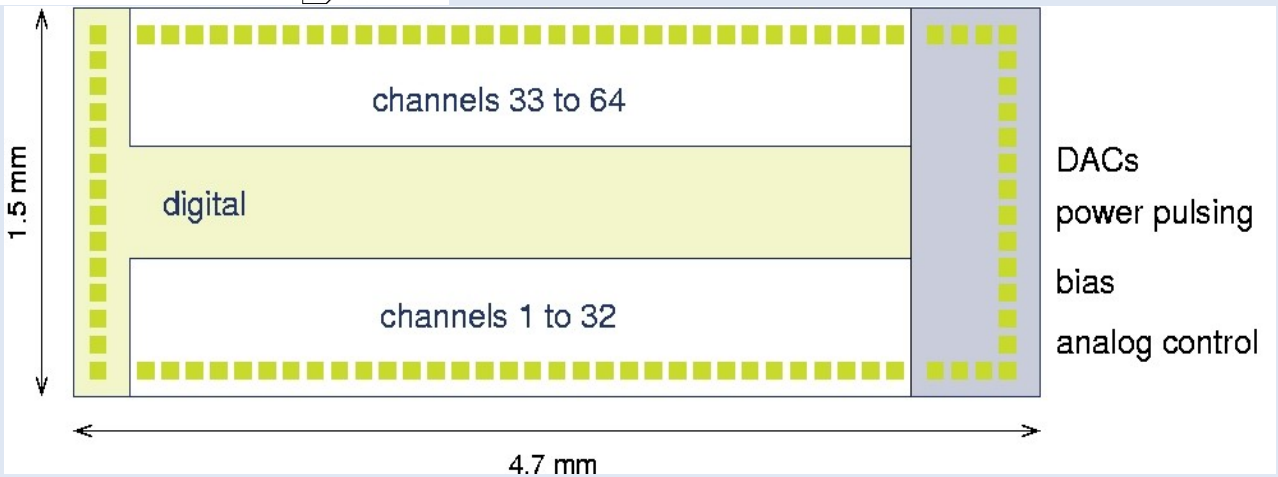
DIRAC ASIC

A new chip with a low threshold for µMEGAS
is under development @IPNL

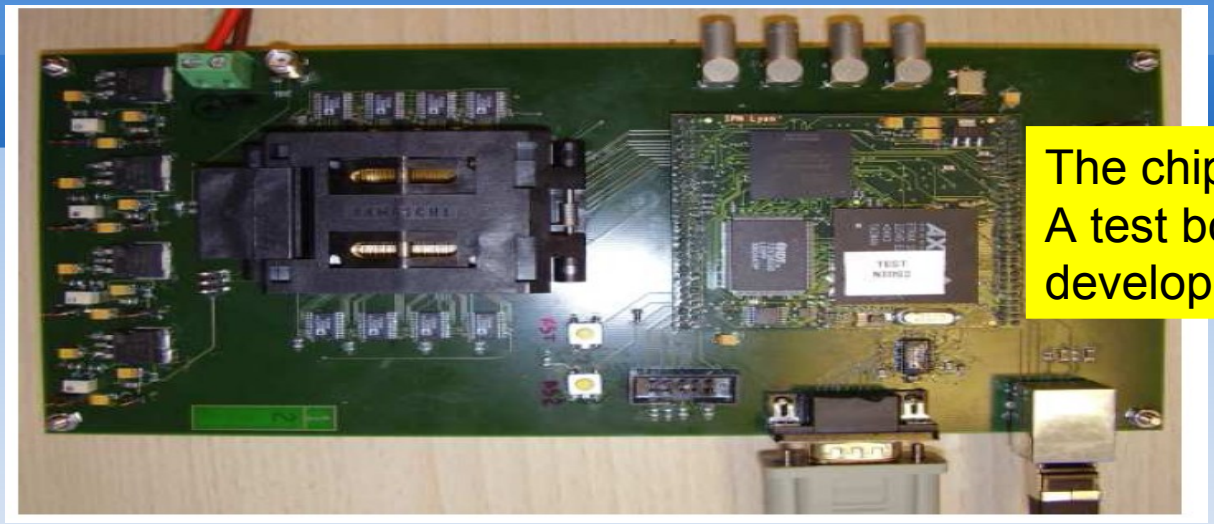


3 DACs (8 bits each)
BCID = 12 bits
memory depth= 8 evts

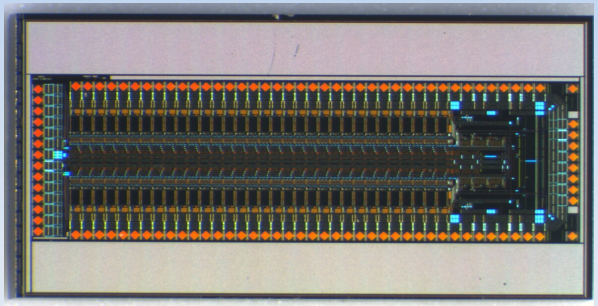
64-ch chip
CMOS tech
power pulsed

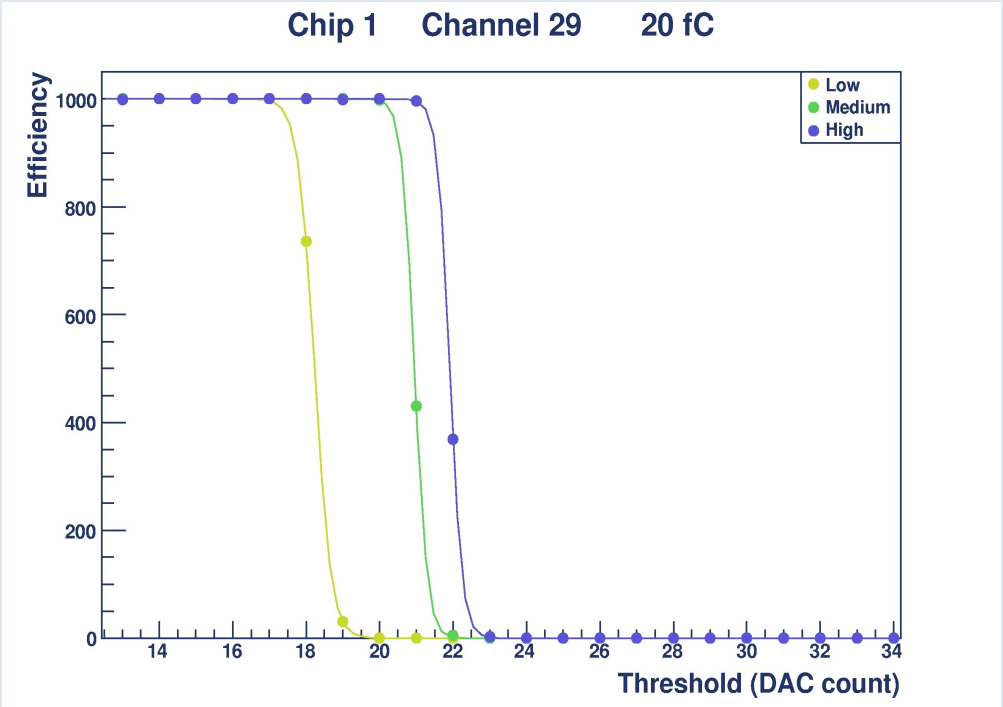


Simple geometry



The chip was designed and produced.
A test board using OPERA DAQ developed @IPNL was used.





First results:
Mode µMEGAS
0.8 fc/DAQ
Resolution < 2.5 fc

Tests and improvement are going on