Status of the Data Concentrator Card and plans for the $\int_{DHCAL}$ DAQ2

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CALICE meeting

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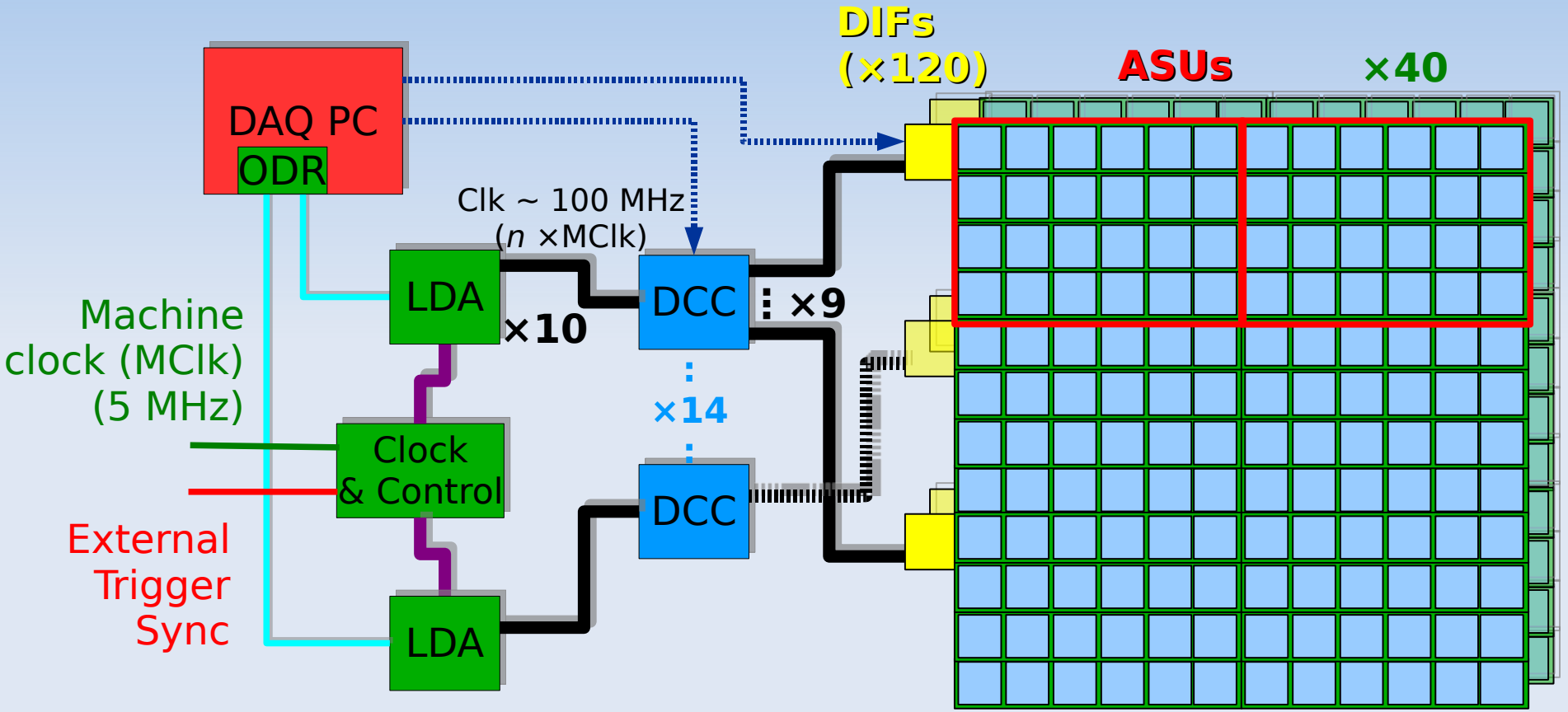
Kyungpook Nat'l U., Daegu, Korea

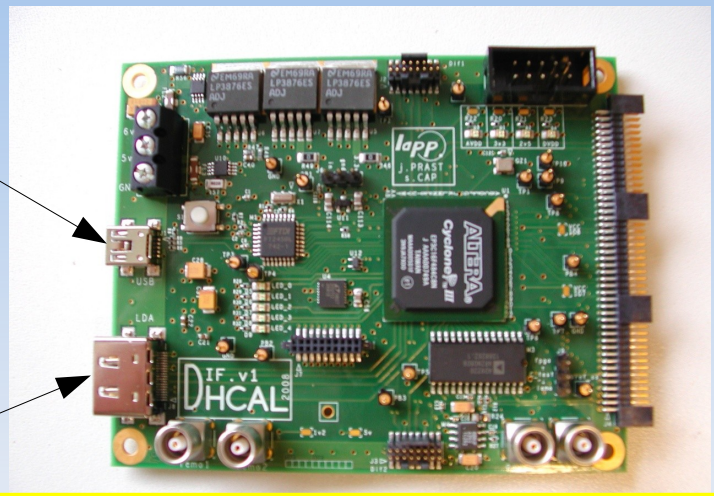
EUDET DAQ2 for the DHCAL



The 1 m² electronics (quick status)

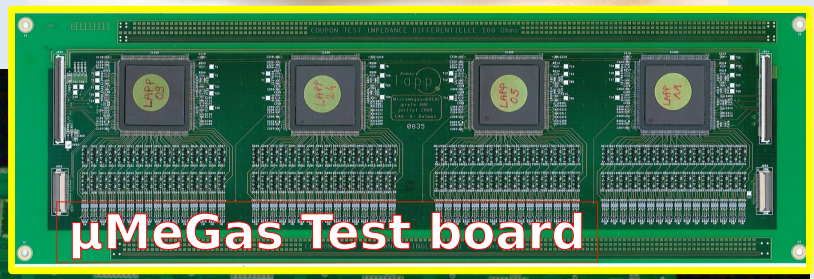
DIF ***Julie Prast & Guillaume Vouters***

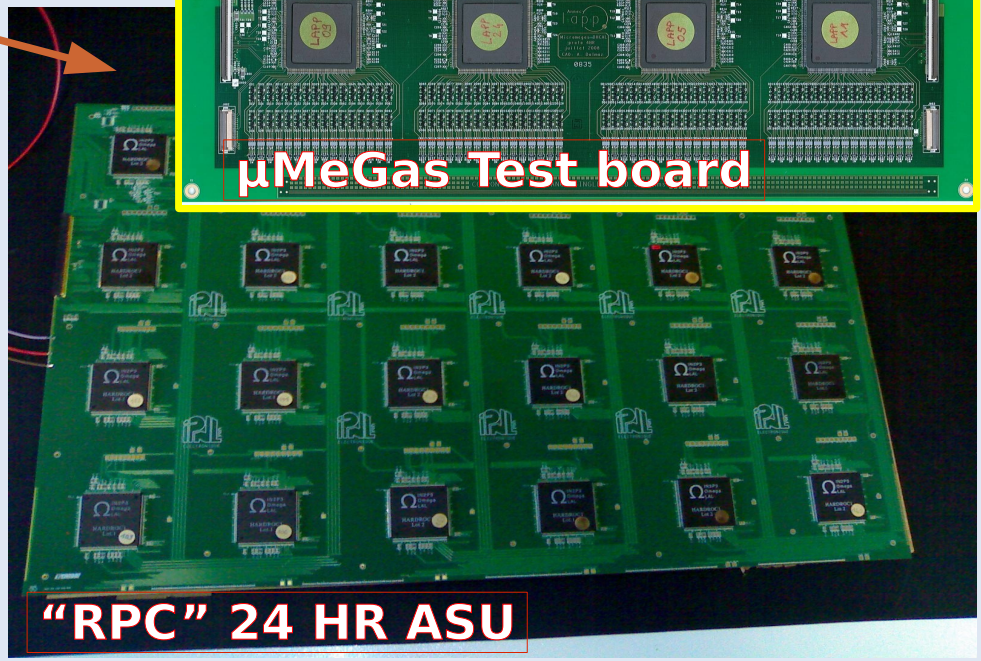
- 10-layer board (6 for signals) designed and prototype produced
- FirmWare & SoftWare operationnal and **tested in beam & cosmics** (with 4 HR µMegas & 24 HR card)



ASUs

- RPC: 50×33.3 cm² (24 HR) boards produced & tested
- µMeGas 32×8 cm² 4 HR produced and tested
- HR1 ASICs used

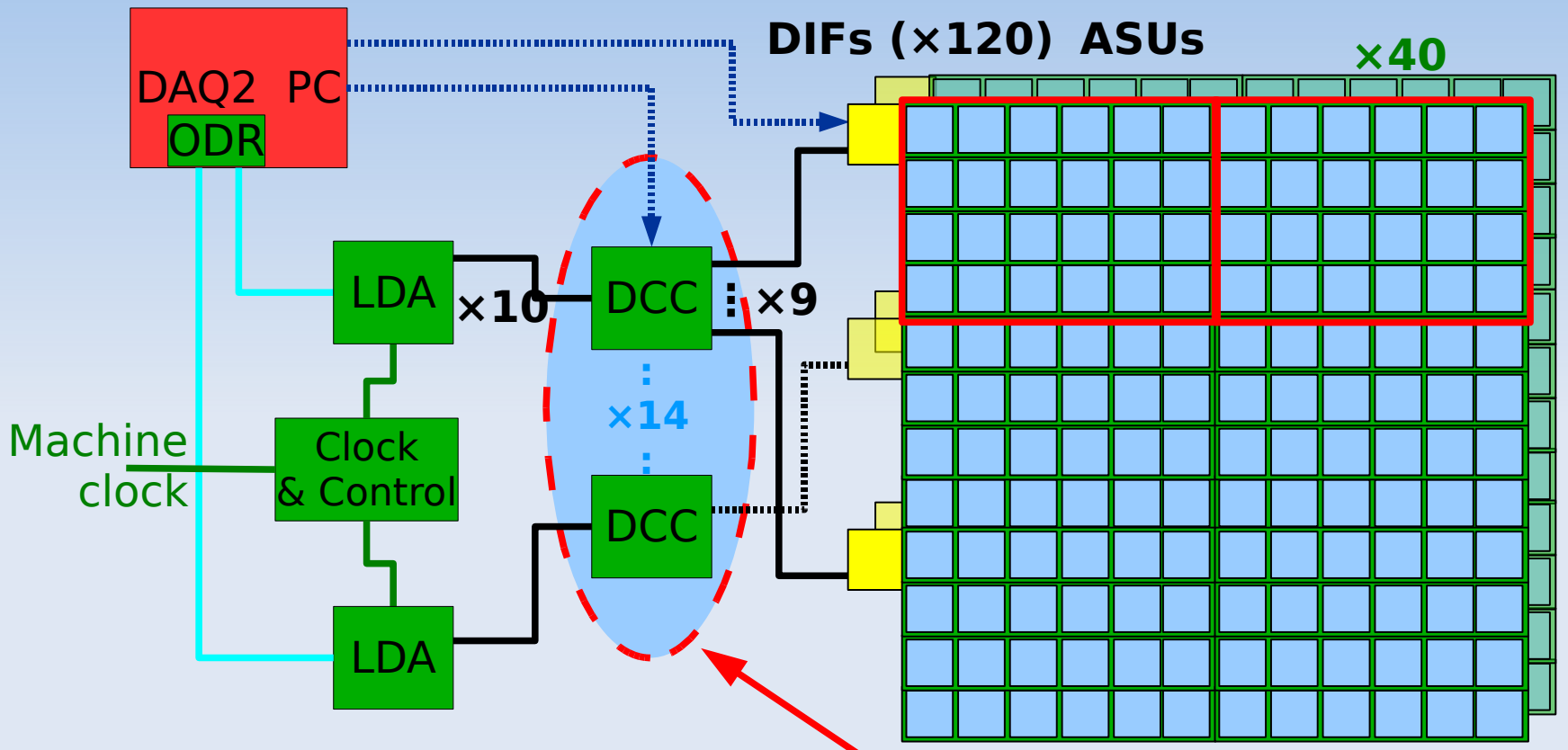




data available:

- µMeGas + 4 HR ASU + DIF TB
  ⇒ not yet analysed
- 48 HR ASU + DIF working in cosmics...

EUDET DAQ2 for the DHCAL



120 DIF → 12 LDA → 4 ODR

120 DIF → 14 DCC → 2 LDA → 1 ODR

Gain for DCC ≤ 1600€

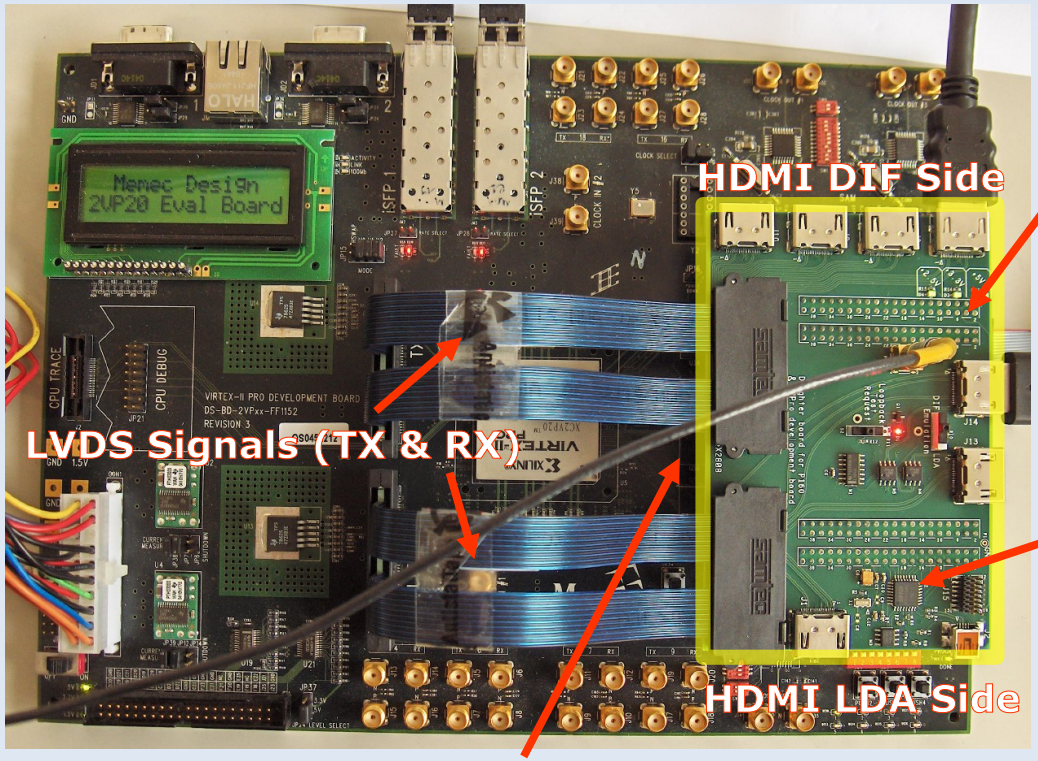
Data Concentrator Card

Franck Gastaldi
Antoine Mathieu

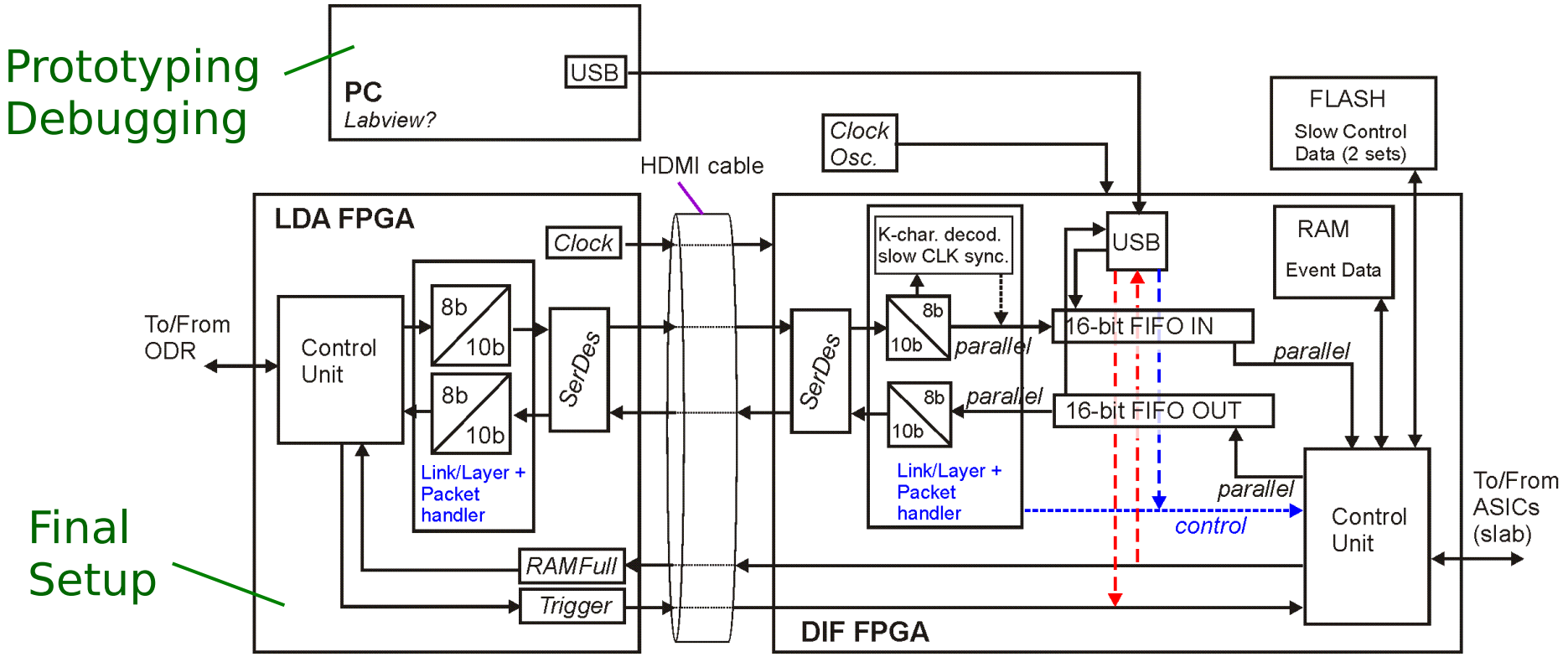
Goals

- Transparency on the path DIF-LDA
- Optimization of flux
- Low cost

- Pre-proto (proto-0)
  - 4 DIFs connections
  - Implantation et tests du code VHDL
- Based on a XILINX evaluation board:
  - 128 Mbits SDRAM
  - Custom Daughter board:
    - HDMI connectors
    - USB blocs



Command Interface - Structure

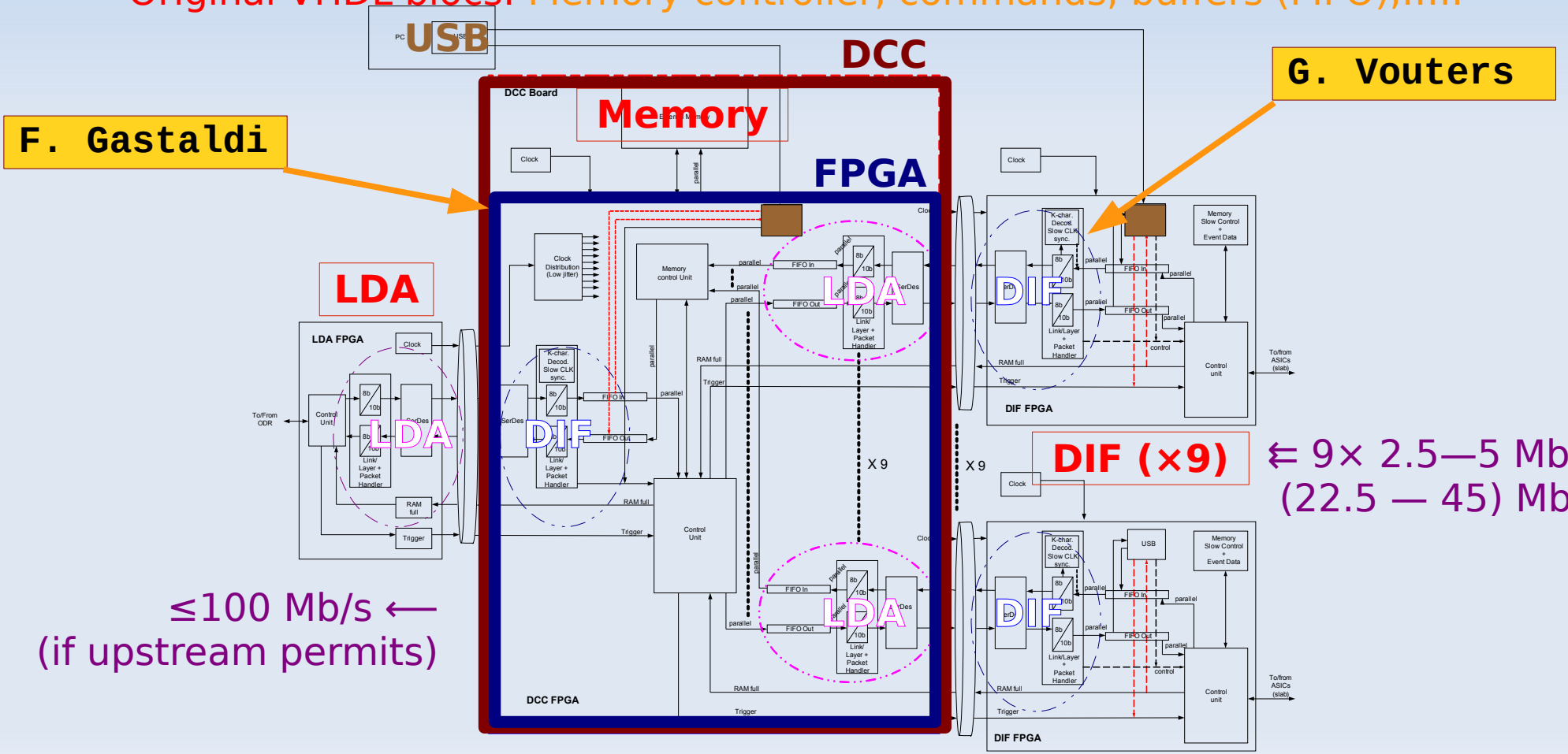


- DIF clock (from LDA): 100MHz (40-120MHz).
- Standard data transfer: 8b/10b channel-coding.
- Trigger/RAMFull: uncoded.

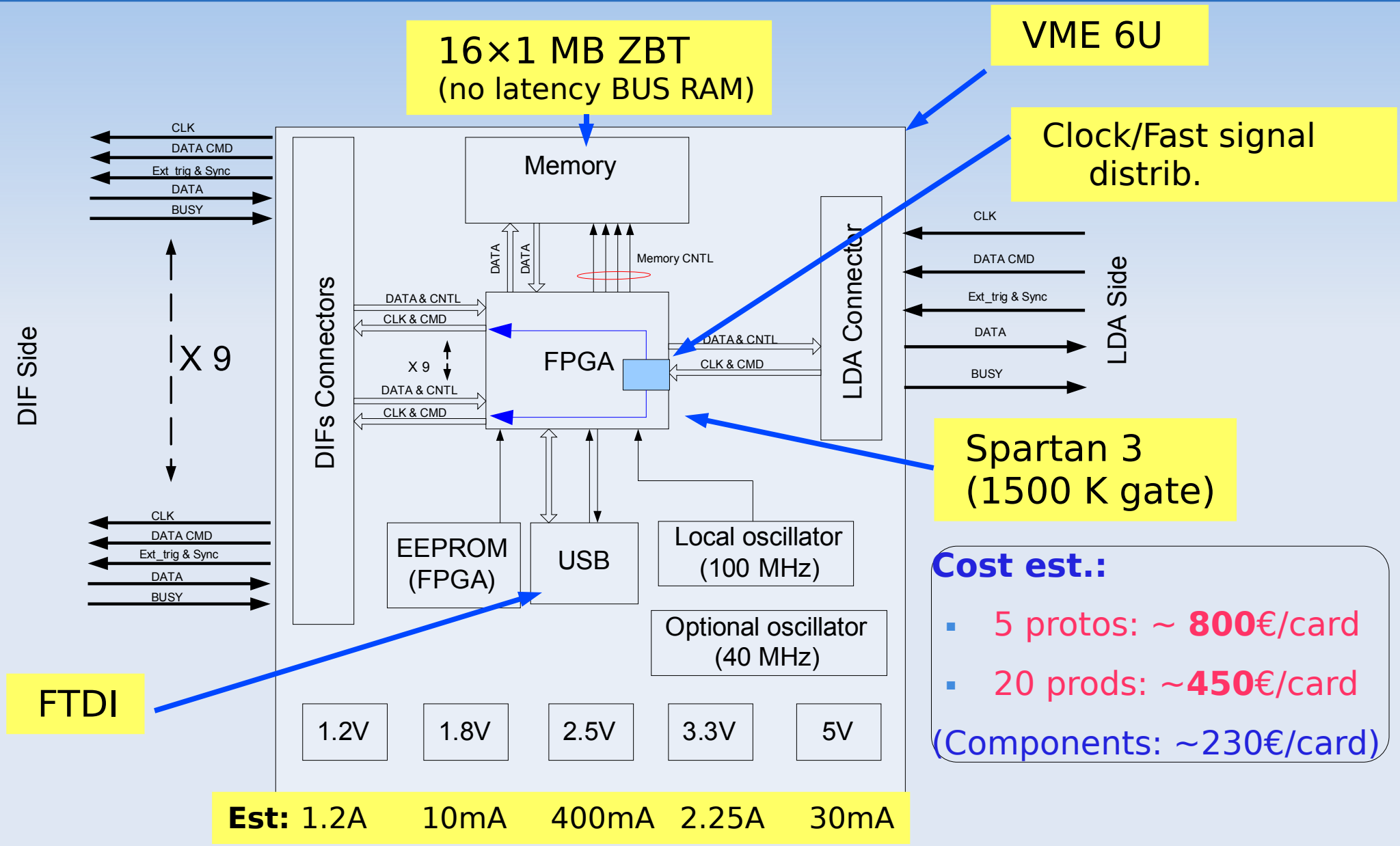
USB interface emulates LDA interface (clock-source: free of choice).

DCC prototype data flux

- **Developments**:
  - Marc Kelly (U. Man) : blocs Ser-Des, coding 8b/10b
  - USB blocs (from Clément Jauffret & Guillaume Vouters)
  - Original VHDL blocs: Memory controller, commands, buffers (FIFO),.....



DCC Proto-1



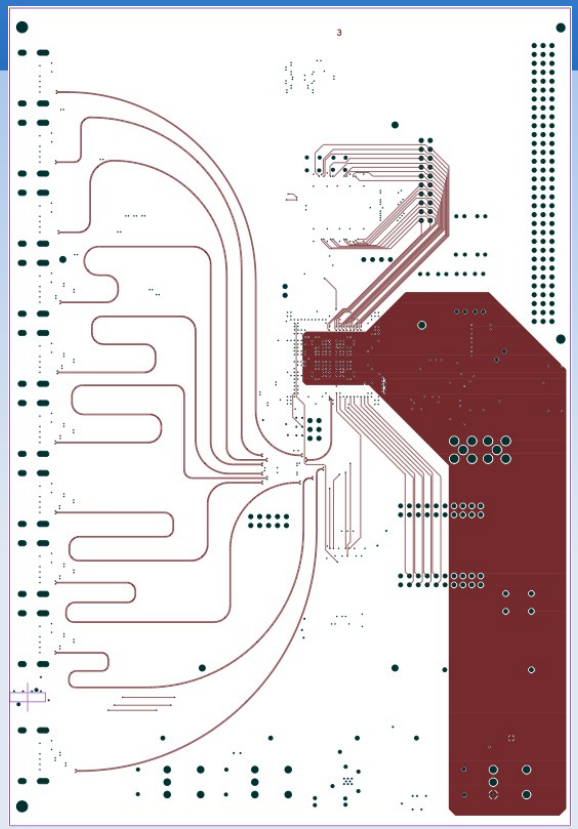
Cost est.:

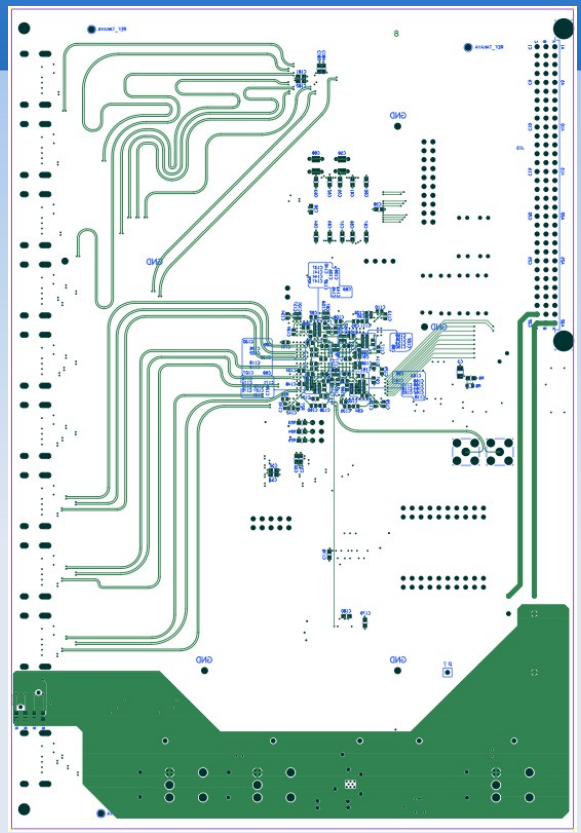
- 5 protos: ~ **800**€/card
- 20 prods: ~**450**€/card

(Components: ~230€/card)

Planning DCC

- February 09:
  - Proto-1
    - 2 PCB received
    - Cabling ⊂ 2 wks





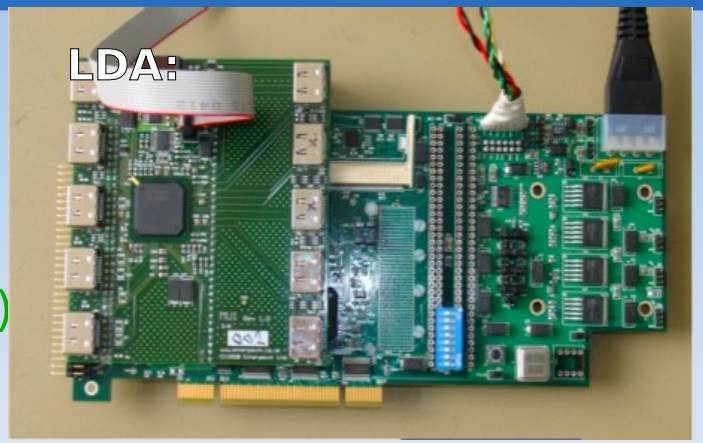
- March- April 09
  - Test of prototype
  - Test bench mounting
  - Validation & ∫ of VHDL blocs (started)
- Mai – June 09 (estimation)
  - Production of boards for the m³

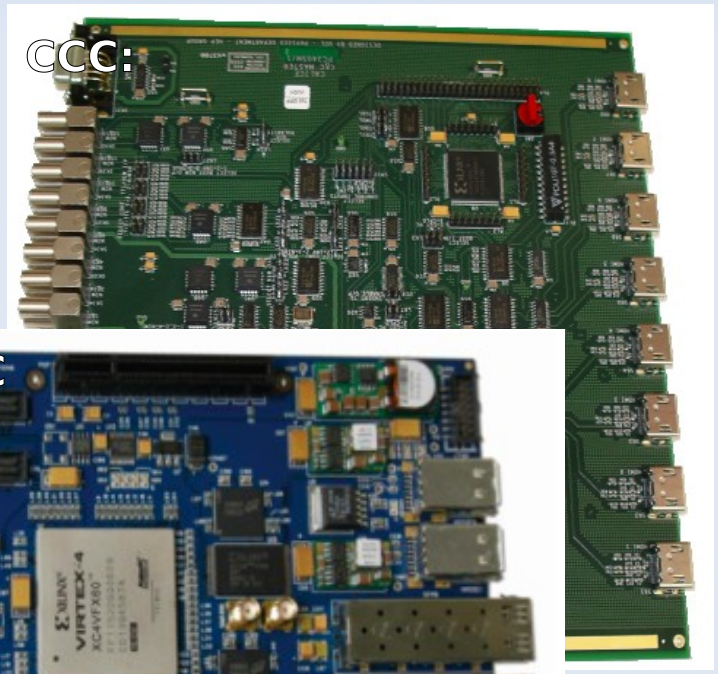
→

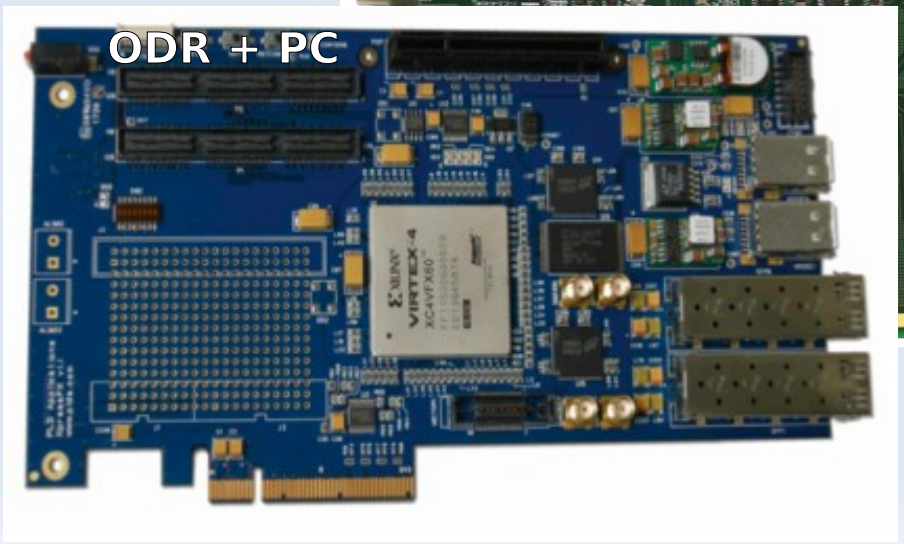
- Looping DCC-DIF / DCC-LDA
- Connection with the DIF (code on DIF: started)

DAQ2 Hardware: status of 12/12/08

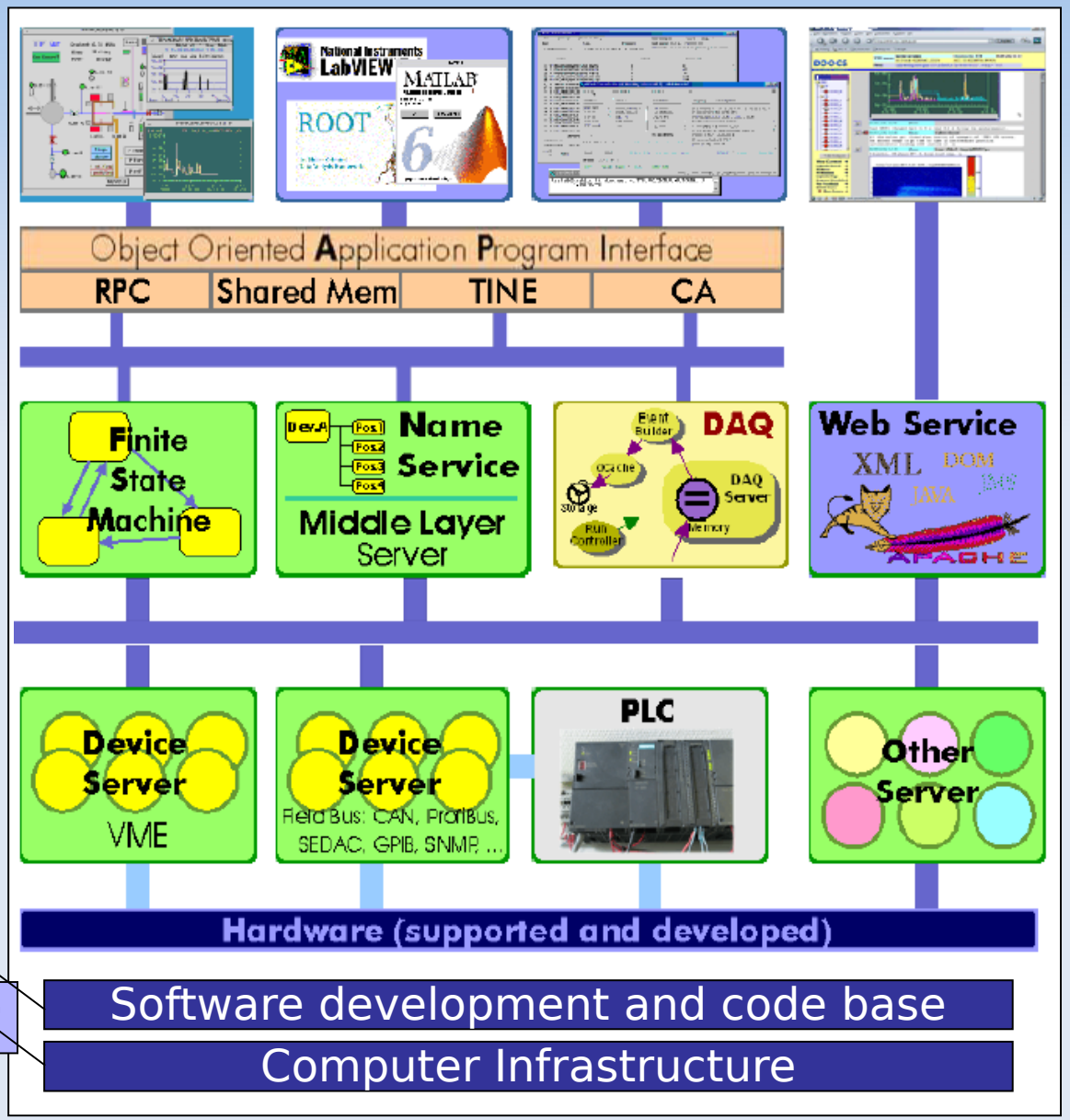
- Components:
  - 1 Proto-DHCAL DIF ✔, ECAL DIF (2 protos) ✔
    - Integration code LDA-DIF on going
  - 1 LDA (HW ✔ **but 8-10 wks** ⚠, FW ongoing)
  - 1 CCC ✔ (2 cards avail., 8 more in prod)
  - 1 ODR v2 + 1 PC DAQ ✔ (mid feb.)
  - 1 proto DCC (march) or proto-0
- HW and protocols: on-going → March ?
- Mars 09 → Jun 09
  - DAQ code DOOCS
  - Integration for a m³







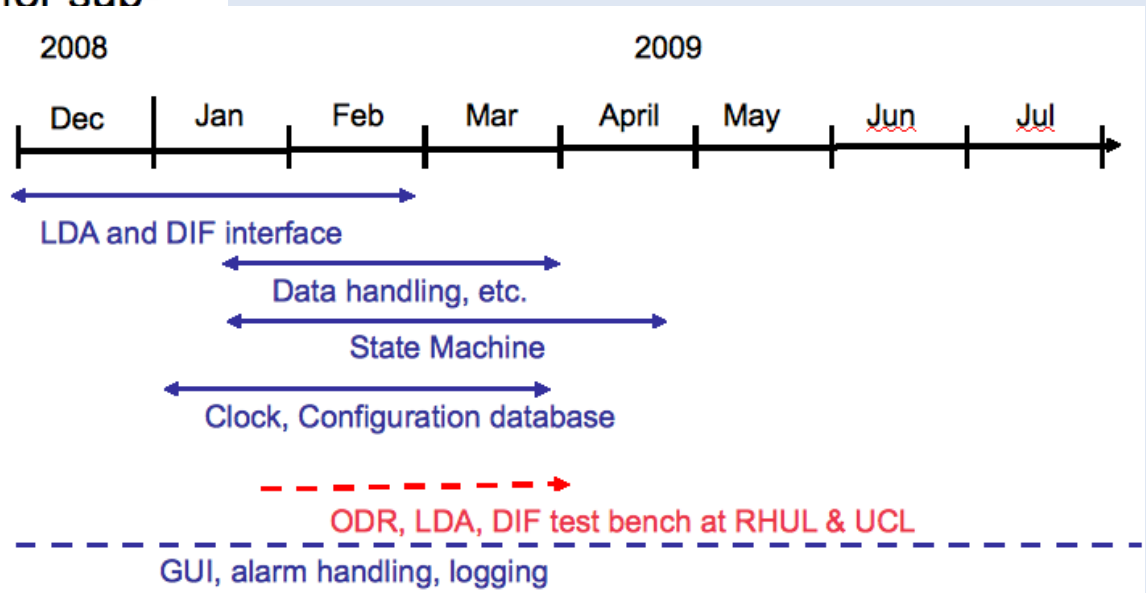
DAQ2 SW components: DOOCS



DAQ2 SW To do's & Timeline

Some essentials

- The components are not integrated in software,
  - LDA / DIF / ASICs
  - Full chain will be available ~Jan/2009.
- No event building & LCIO converting
  - Data are saved to local disk in raw format;
  - Just provide interfaces in the framework;
  - More flexible way to leave them free for sub-detector groups to develop.



DAQ2 test benches

- Meeting 12/12/2008 in DESY: needs of various groups
- 1 bench in LLR: **D. Decotigny**
  - DAQ PC + ODRv2 end-February
    - now: PC + DCC pre-proto
      - USB access to DCC proto-0 ✔
      - DCC auto-sending (DIF/LDA)
    - scripting (python ?)
      - to be used for ECAL tests (See D. Jeans talk)
    - test with USB connection on DCC & DIFs
  - test readout with ODR + LDA (or emul) of a few DIF's
  - integration of all DOOCS components
    - LCIO data writing
    - Event display
    - Database integration with LCDB (MySQL based)
    - Slow Control

Data Flow & expected rates

N DIF/LDA	N DIF/DCC	LDA-DIF Dclk [MHz]	LDA-DIF FLUX [MB/s]	LDA Dclk [MHz]	LDA FLUX [MB/s]	ODR FLUX [MB/s]	Disk Flux [MB/s]
10	**9**	**80**	*10*	**1000**	*125*	**1000**	**170**
Detector	**DHCAL**	Evt Size	Mem Size	ASIC Dclk [MHz]	ASIC FLUX [MB/s]		
		20 B	**128**	**2,5**	0,31		
Mode	Calib/Noise Single	Calib/noise Burst	TB Single	TB Burst	Demo		
N ASIC/DIF	**48**	48	**6**	6	6		
ASIC	20 B	2 560 B	20 B	2 560 B	2 560 B	LC-DET-2004-029	
R/O time 1	*64 µs*	*8 192 µs*	*64 µs*	*8 192 µs*	*8 192 µs*	*Mean*	4,8
R/O time ALL	***3 072 µs***	***393 216 µs***	***384 µs***	***49 152 µs***	***49 152 µs***	*sigma*	2,6
DIF	960 B	122 880 B	120 B	15 360 B	15 360 B	+3σ /√128	5,49
R/O time	*96 µs*	*12 288 µs*	*12 µs*	*1 536 µs*	*1 536 µs*		
LDA w/o DCC	9 600 B	1228 800 B	1 200 B	153 600 B	153 600 B		
R/O time	*77 µs*	*9 830 µs*	*10 µs*	*1 229 µs*	*1 229 µs*		
DCC	8 640 B	1 105 920 B	1 080 B	138 240 B	138 240 B		
R/O time	*864 µs*	*110 592 µs*	*108 µs*	*13 824 µs*	*13 824 µs*		
LDA w/ DCC	86 400 B	11 059 200 B	10 800 B	1 382 400 B	1 382 400 B		
R/O time	*691 µs*	*88 474 µs*	*86 µs*	*11 059 µs*	*11 059 µs*		
ODR	17 280 B	2 211 840 B	2 160 B	276 480 B	276 480 B		
1000MB/s	*17 µs*	*2 212 µs*	*2 µs*	*276 µs*	*276 µs*		
Disk	17 280 B	2 211 840 B	2 160 B	276 480 B	276 480 B		
170MB/s	*102 µs*	*13 011 µs*	*13 µs*	*1 626 µs*	*1 626 µs*		
Max R/O time	***3 072 µs***	***393 216 µs***	***384 µs***	***49 152 µs***	***49 152 µs***		
Min Freq	0,33 kHz	0,00 kHz	2,60 kHz	0,02 kHz	0,02 kHz		
Min. evts Freq		0,33 kHz		2,60 kHz	2,60 kHz		

Acq Mode

Limiting Factor

Expected speed

Number of hit ASICs for 100 GeV π

"Overkill for RPC"

Summary

- All HW component for the DAQ are now available
  - some need extra prod (LDA, CCC)
  - DCC is advancing well according to planning
    - test prod this month (3 wks)
- FW: on-going everywhere
  - DHCAL DIF OK for USB but needs integration of DIF-LDA blocks
  - Effort of DIF Task force to write modular code on-going
  - LDA & DCC in intensive development
  - Protocol definition crystallising
- SW: Almost full skeleton working
  - integration of HW started
  - needs implementation in a real test bench with real objects (in part. ASICs) → @ UCL and LLR soon
- Good hope for full working system at end of spring → *use in June TB ?*

DCC pre-proto